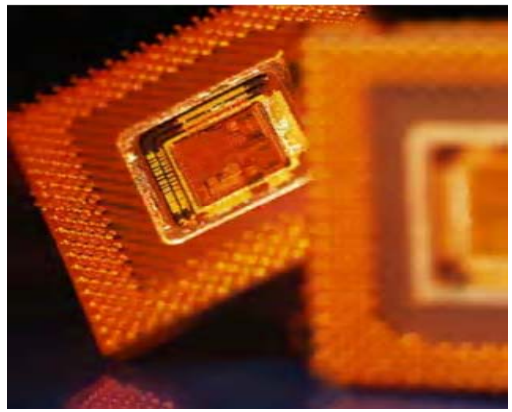
An Overview of Microelectronic Fabrication



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Outline

- IC History & Trend
- Why Do We Study Integrated Circuit Process?
- Silicon Material
- How To Make Wafer?
- Overview of IC Fabrication Process



1. IC History & Trend

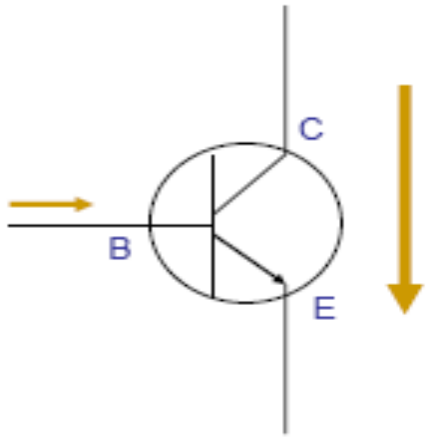
1-1. Vacuum Tube

■ **Primary Purpose : Electrical Switch**

■ **Bonus : Amplifier**

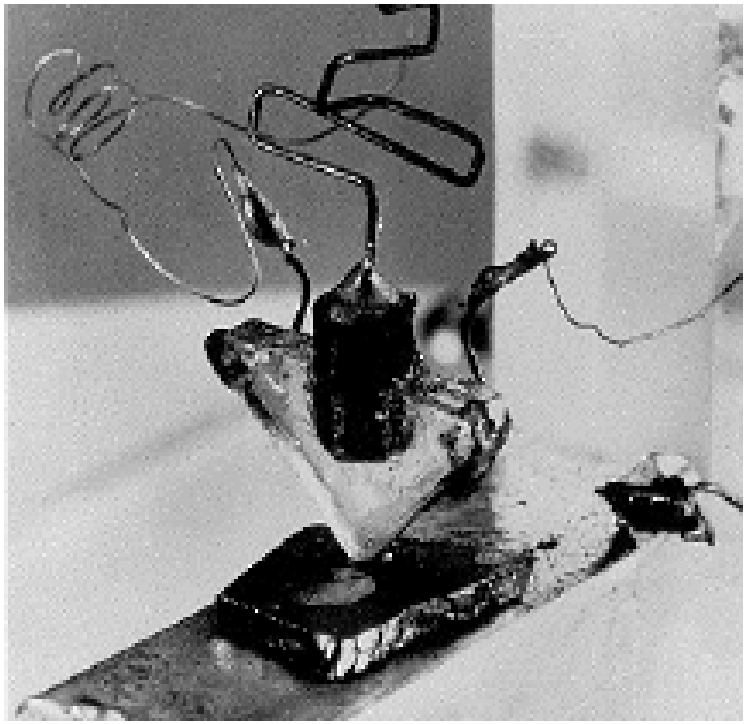


Vacuum Tube Amplifier



Semiconductor Transistor Symbol

1-2. Invention of the Transistor



World the 1st Transistor in 1948

■ Motivation

◇ **To replace mechanical switches in telephone line exchangers. It was invented in Bell Lab.**

■ Nobel Prize Went To

◇ William Shockley

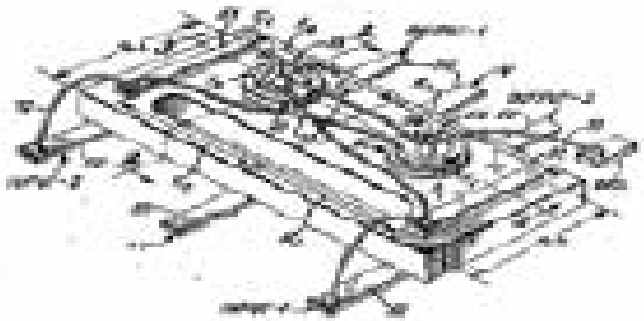
◇ Walter Brattain

◇ John Bardeen

1-3. Invention of the Integrated Circuit


United States Patent

Kilby



■ **1959**

◇ **Jack Kilby (TI) invented the monolithic integrated circuit.**

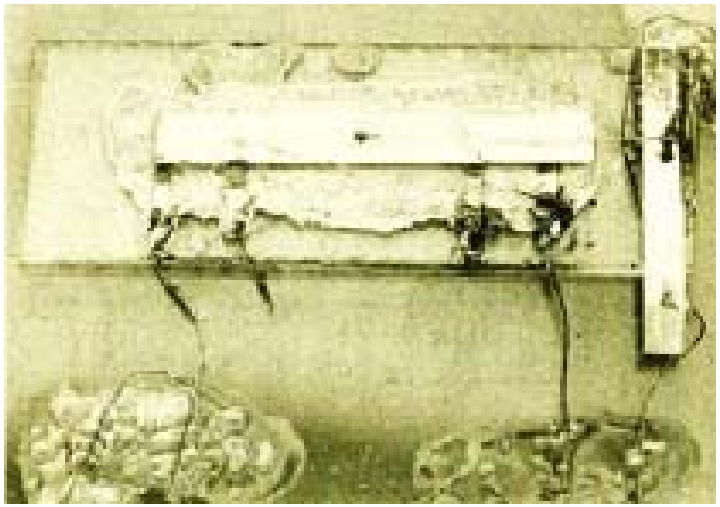
■ **Design**

was improved by Robert Noyce (Fairchild Semiconductor) to produce planar technology.



1-3. Invention of the Integrated Circuit (cont.)

1958: 1st IC

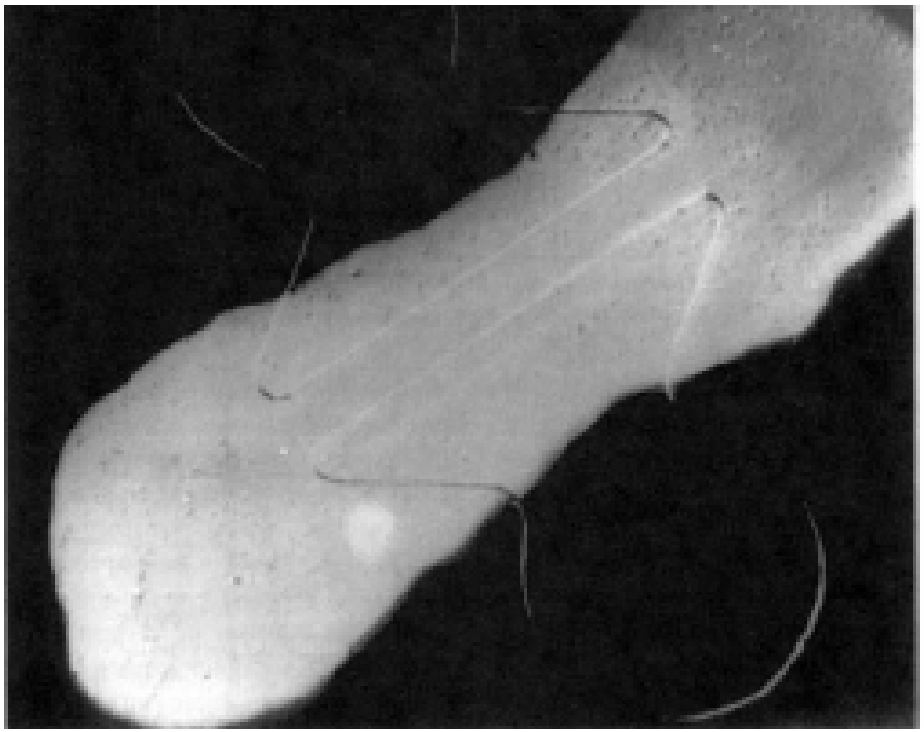


Jack S. Kilby

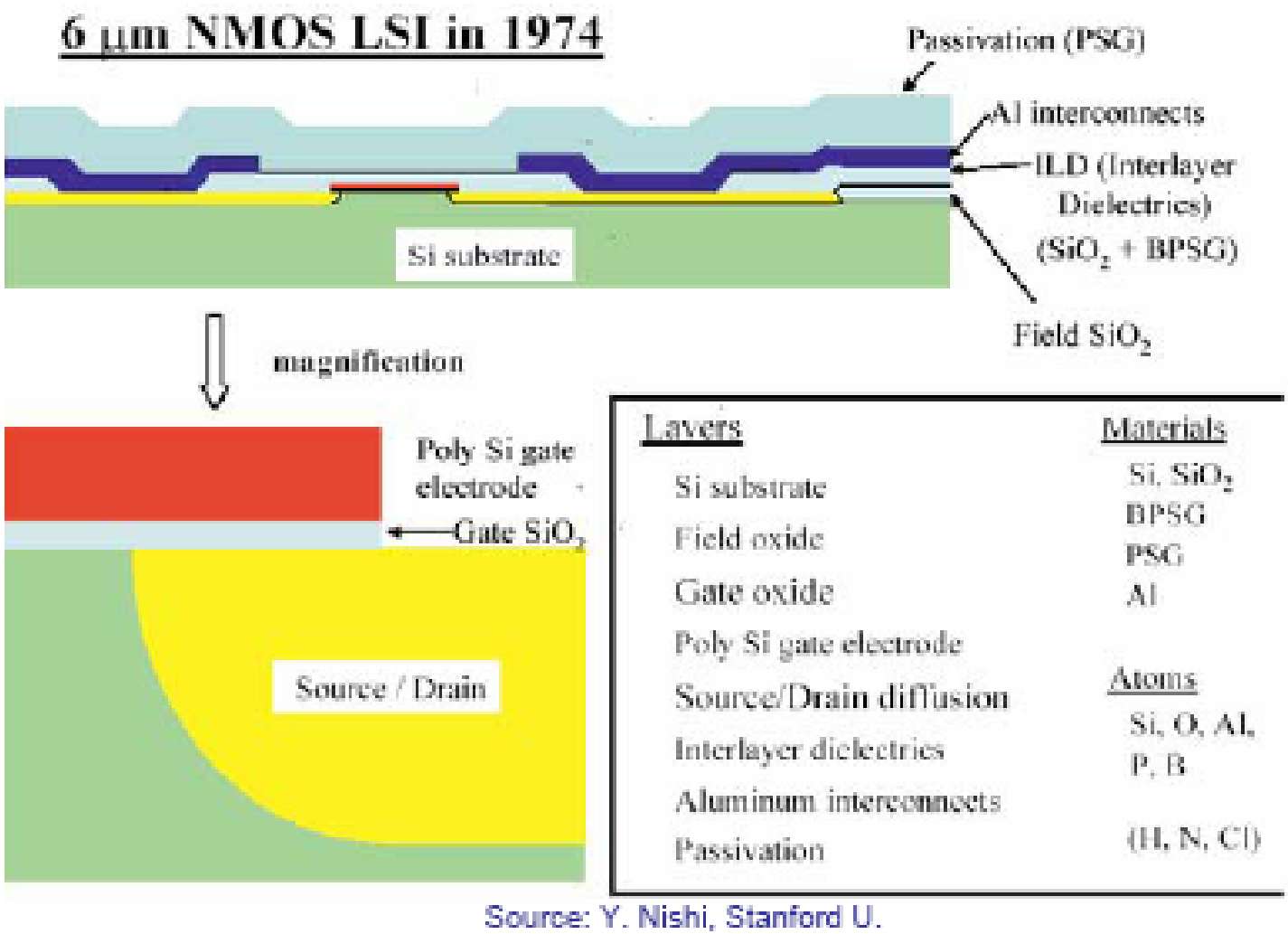


1-4. The 1st MOSFET

1960: 1st MOSFET by D. Kahng and M. Atalla

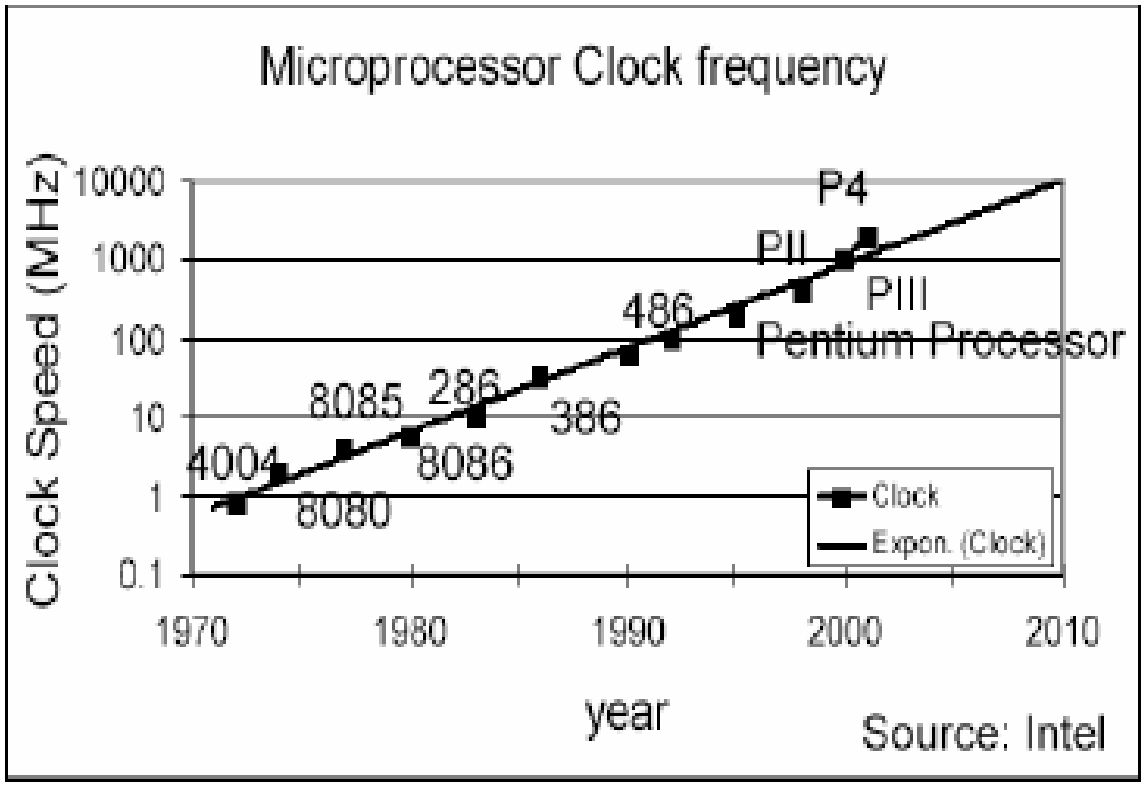


1-5. Large Scale Integration (LSI)



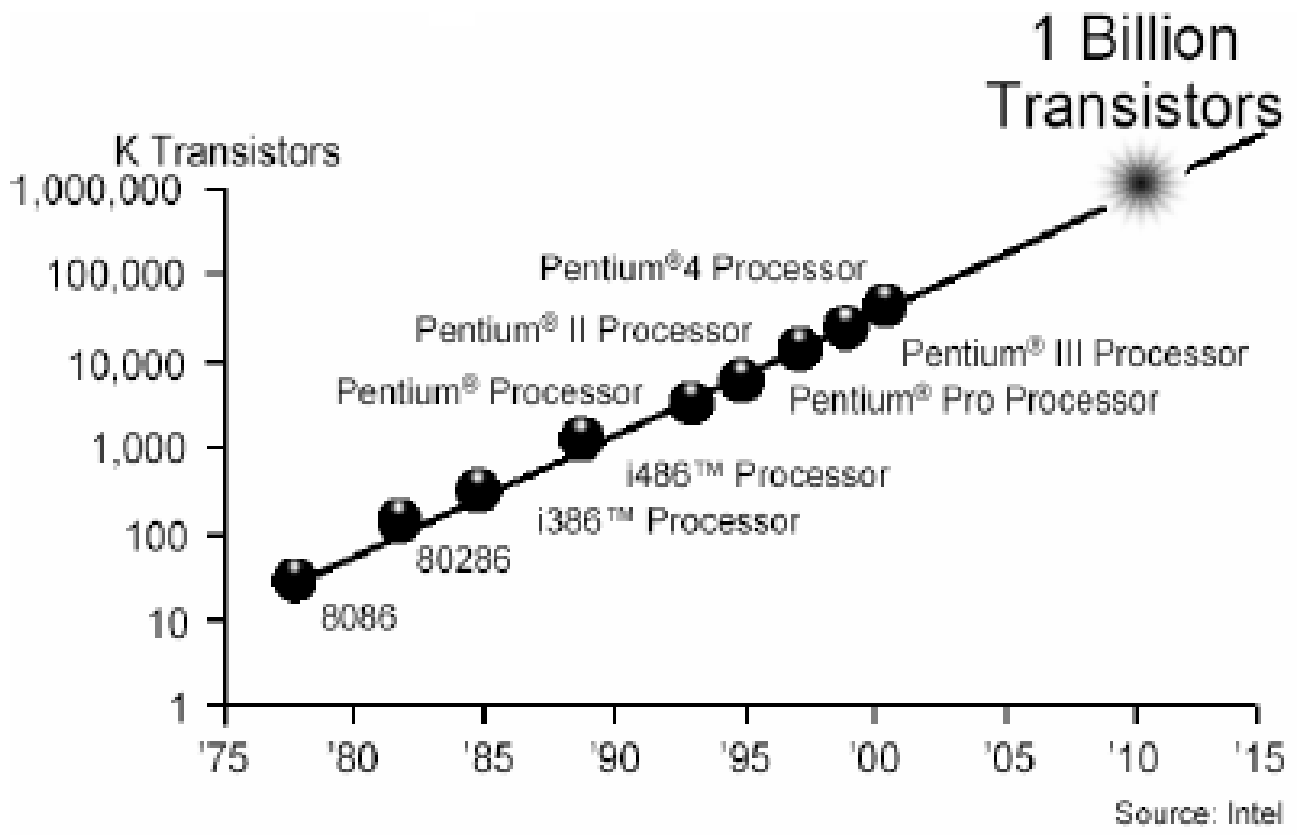
Source: Y. Nishi, Stanford U.

1-6. 마이크로 프로세서 클럭속도 변화



- 3년마다 2배씩 증가
- 2010년에 클럭 속도 10GHz 예상

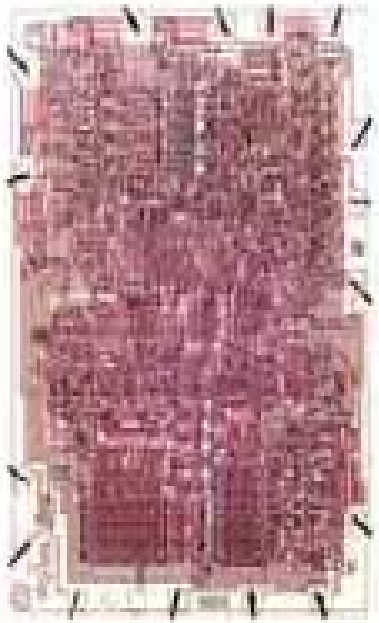
1-7. 마이크로 프로세서 클럭속도 변화



- 18개월마다 2배씩 증가 – "무어의 법칙"
- 2010년에 칩당 10억개 트랜지스터 예상

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1-8. 트랜지스터 수 / 칩 비교

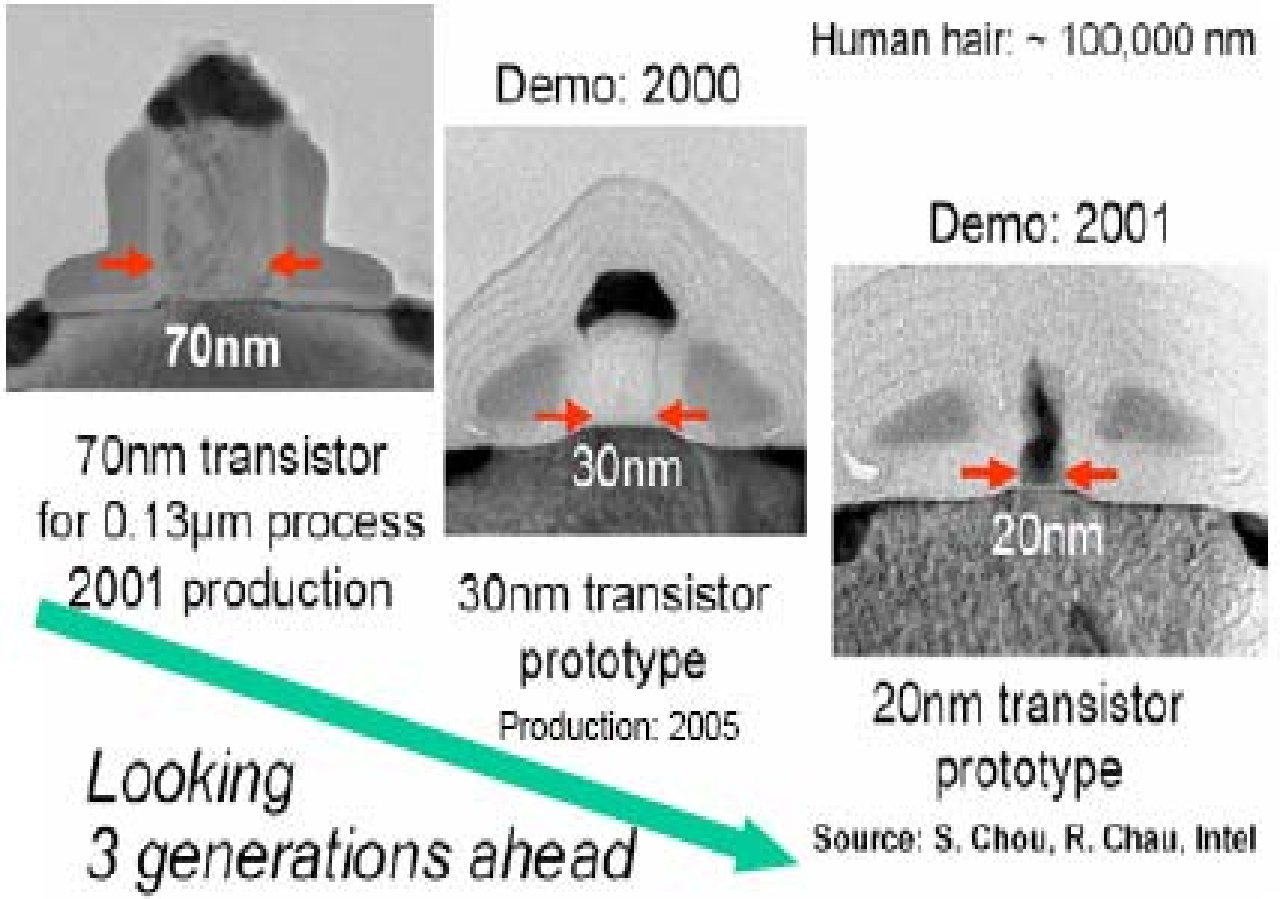




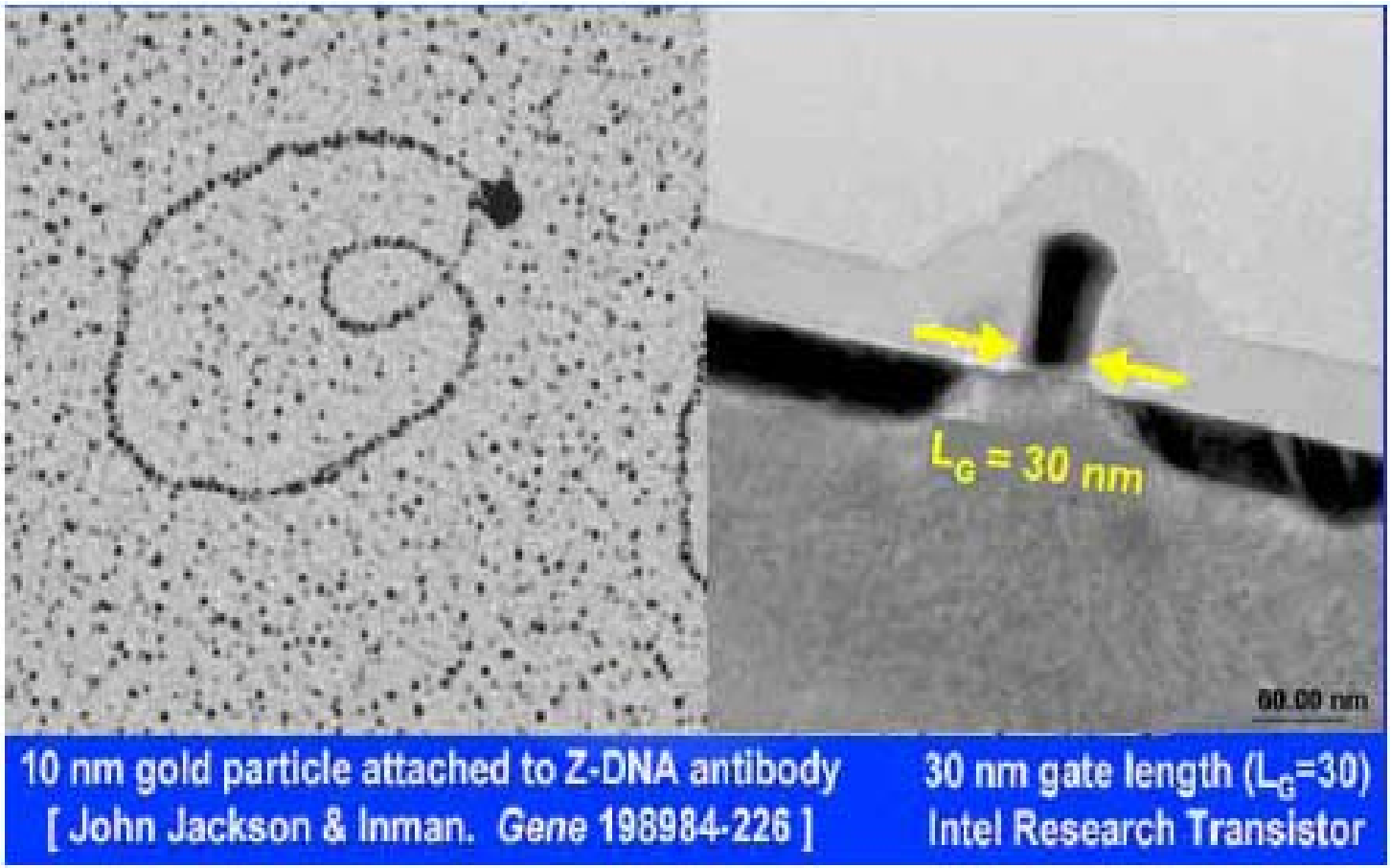
- Intel 4004 1MHz (1971년)
- 2.3천 트랜지스터 - 191개/mm²

- Intel P4 533MHz (2002년)
- 55백만 트랜지스터 - 376,712개/mm²

1-9. 트랜지스터 크기변화



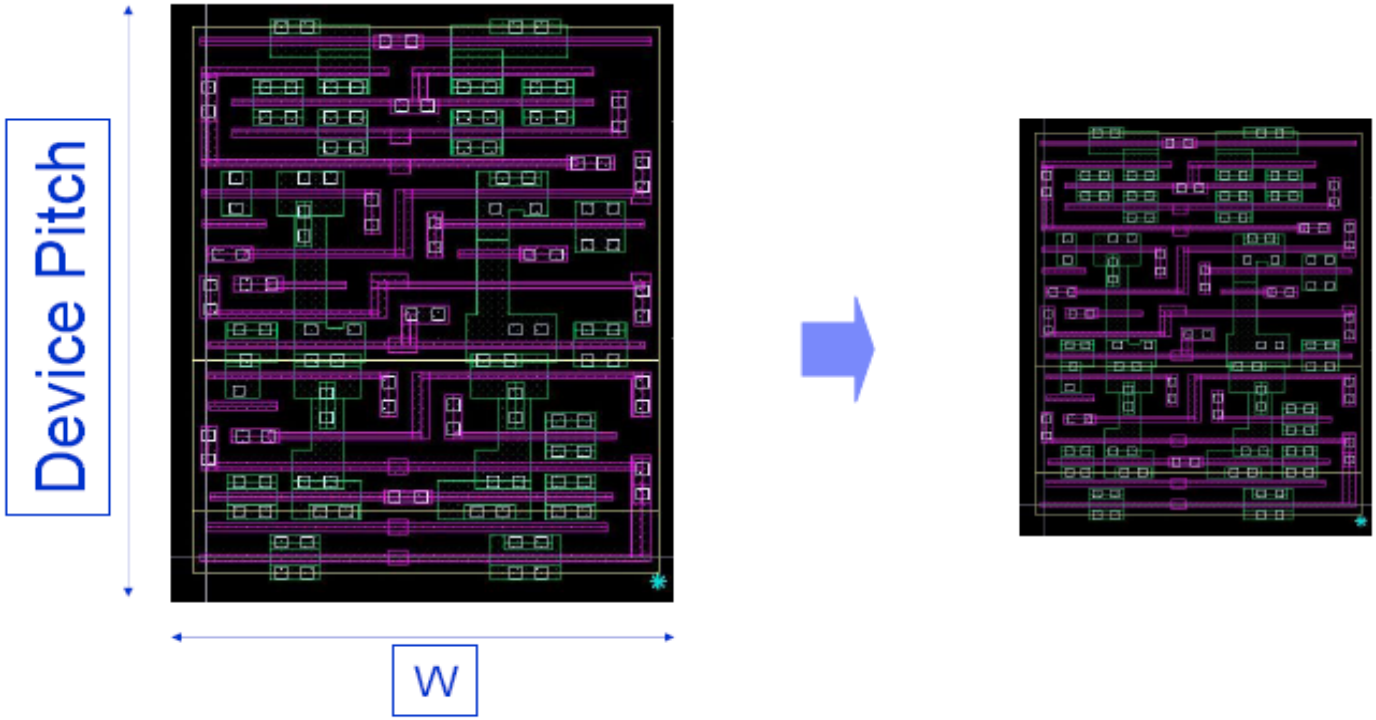
1-10. 트랜지스터 크기비교



● 트랜지스터 하나의 크기가 DNA 크기에 근접

1-11. CMOS Density: Moore's Law





- 30% Reduction in W and device pitch
  - 50% area reduction
  - 2X device/area (every 2 years)



2. Why Do We Study IC Process

2-1. Memory vs. Non-memory

구분	메모리	비메모리
기능	정보의 기록/저장기능	정보의 제어/논리/연산기능
주요제품	DRAM/SRAM/FLASH MEMORY	CPU/자동제어/주문형반도체
응용분야	컴퓨터 및 주변기기	정보통신/컴퓨터/디지털가전/ 네트워크/인터넷시스템
사업특성	소품종 대량생산/호불황기 변동급격	다품종소량생산/호불황기 변동완만
세계시장규모	'01년 : 249억불 '02년 : 271억불	'01년 : 1,141억불 '02년 : 1,134억불
대표업체	삼성/하이닉스/마이크론/인피니온	TSMC/UMC/인텔
국내업체 시장점유율	'01년 : 삼성 19%, Hynix 7% '02년 : 삼성 22%, Hynix 7%	'01년 : 국내업체 1.6% 점유 '02년 : 국내업체 2.2% 점유
수출입현황	'01년 : 62억불 수출 초과 '02년 : 81억불 수출 초과	'01년 : 75억불 수입 초과 '02년 : 89억불 수입 초과

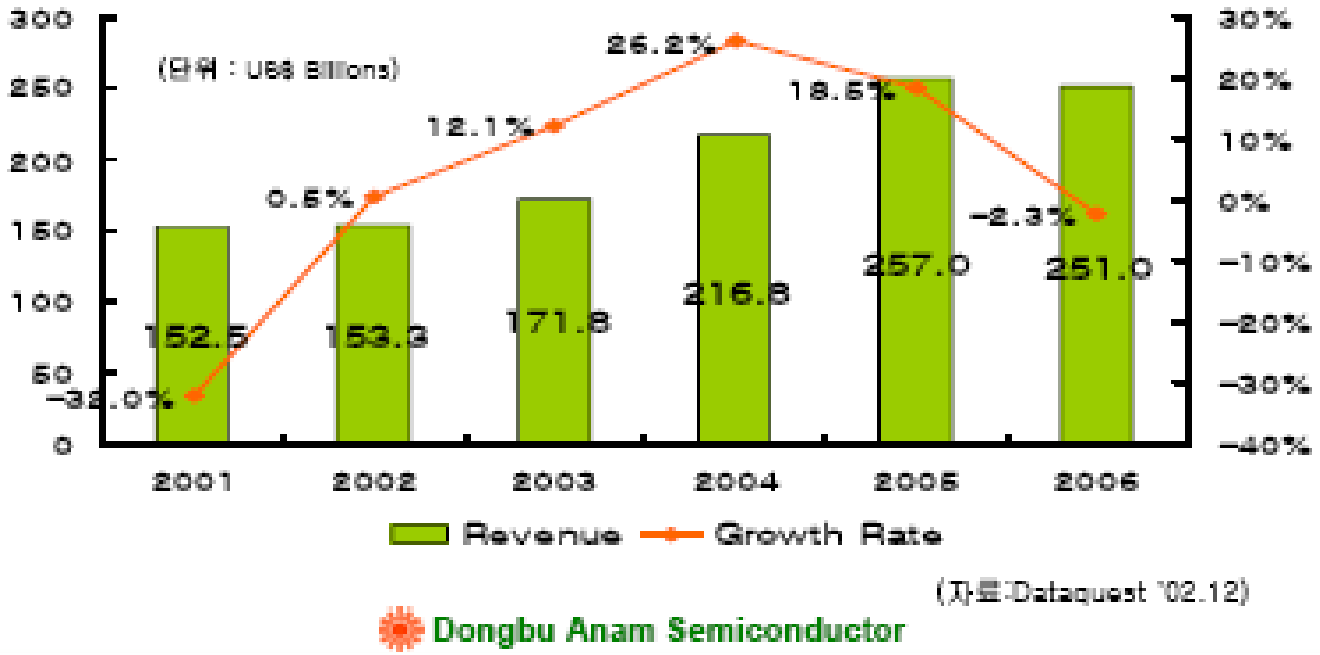
Dongbu Anam Semiconductor

2-2. Prediction of Semiconductor Market

❒ 세계 반도체 시장은 '03년 하반기 이후 회복 시작 → '06년까지 연평균 13.1% 성장 전망

❒ 2003년 시장 전망

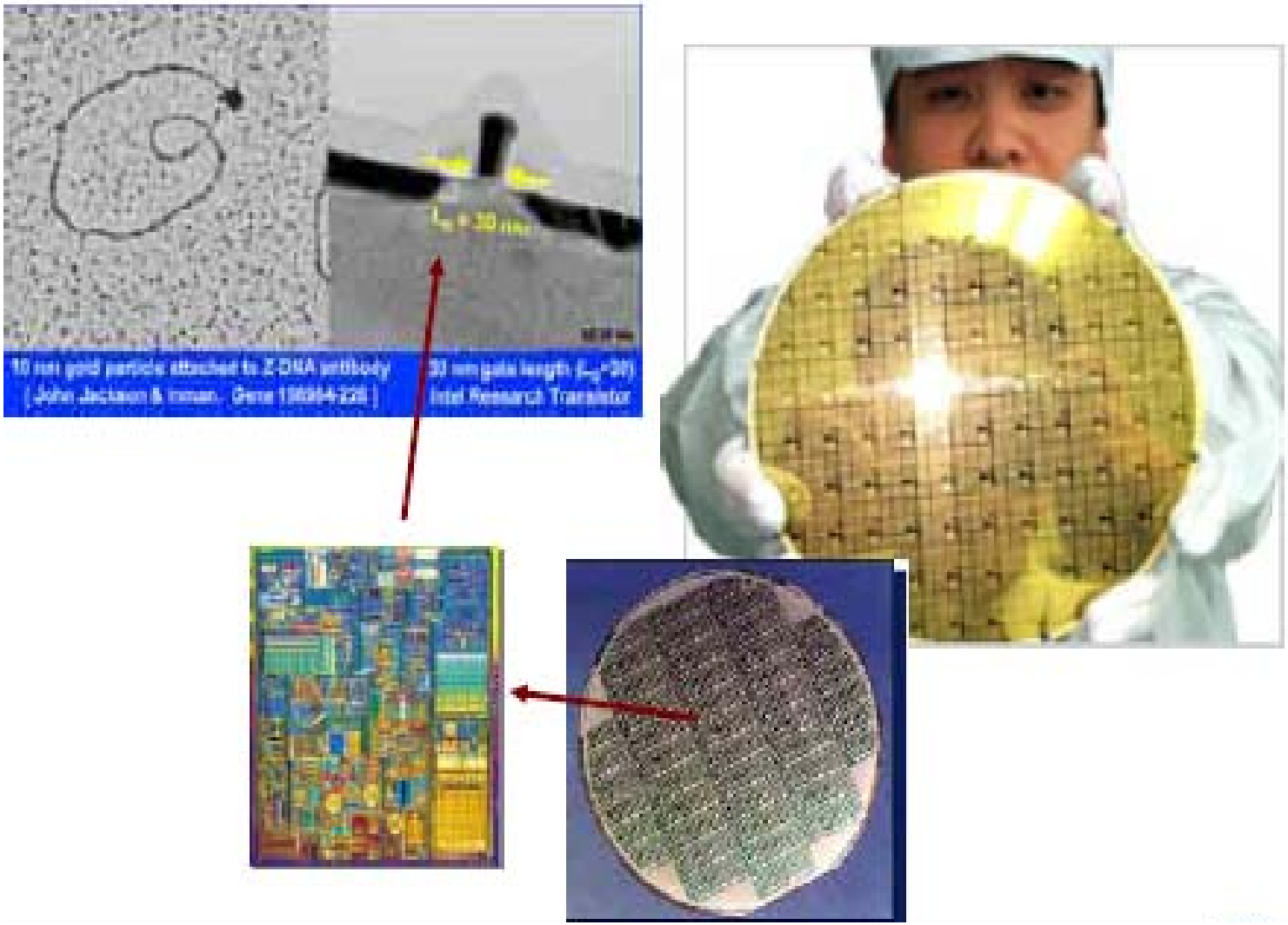
	2002년	2003년
• Revenue	0.5%	12%
• Capital Spending	– 37%	15%
• Wafer Fab Equipment	– 33%	16%
• P&A Equipment	– 23%	25%



(자료:Dataquest '02.12)

Dongbu Anam Semiconductor

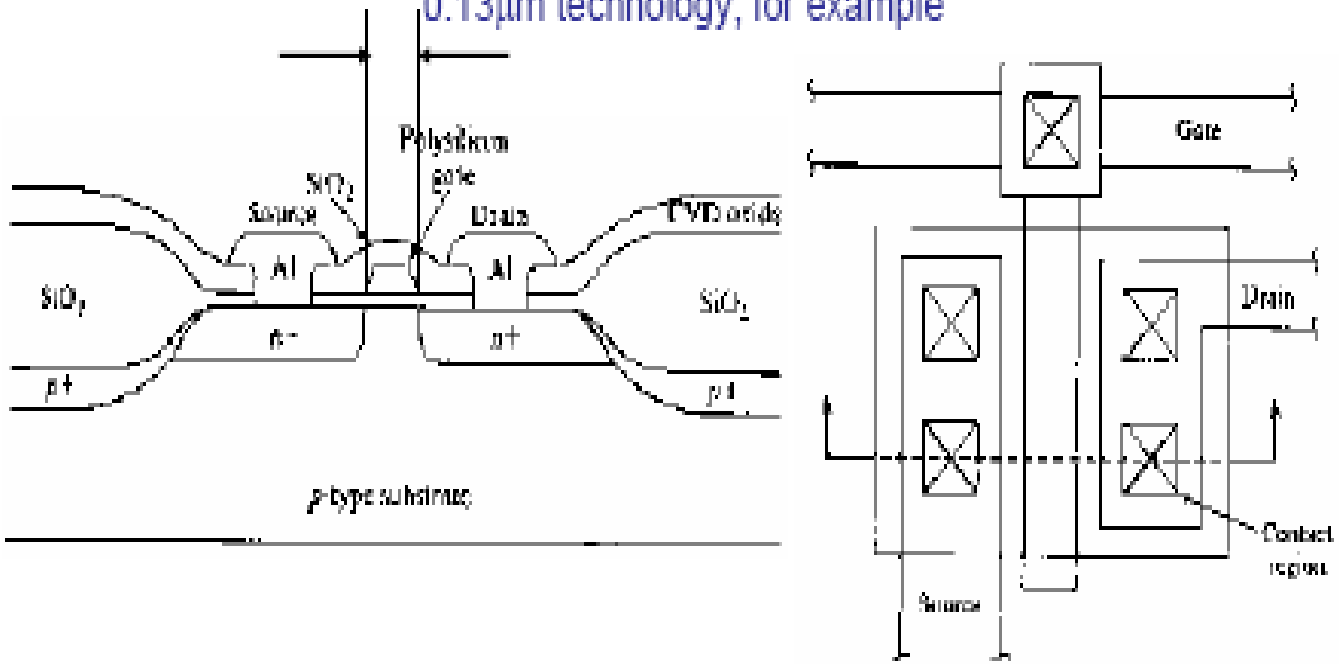
2-3. Semiconductor Wafer Technology



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2-4. A Single Transistor (NMOS)

0.13μm technology, for example



Cross-Sectional View

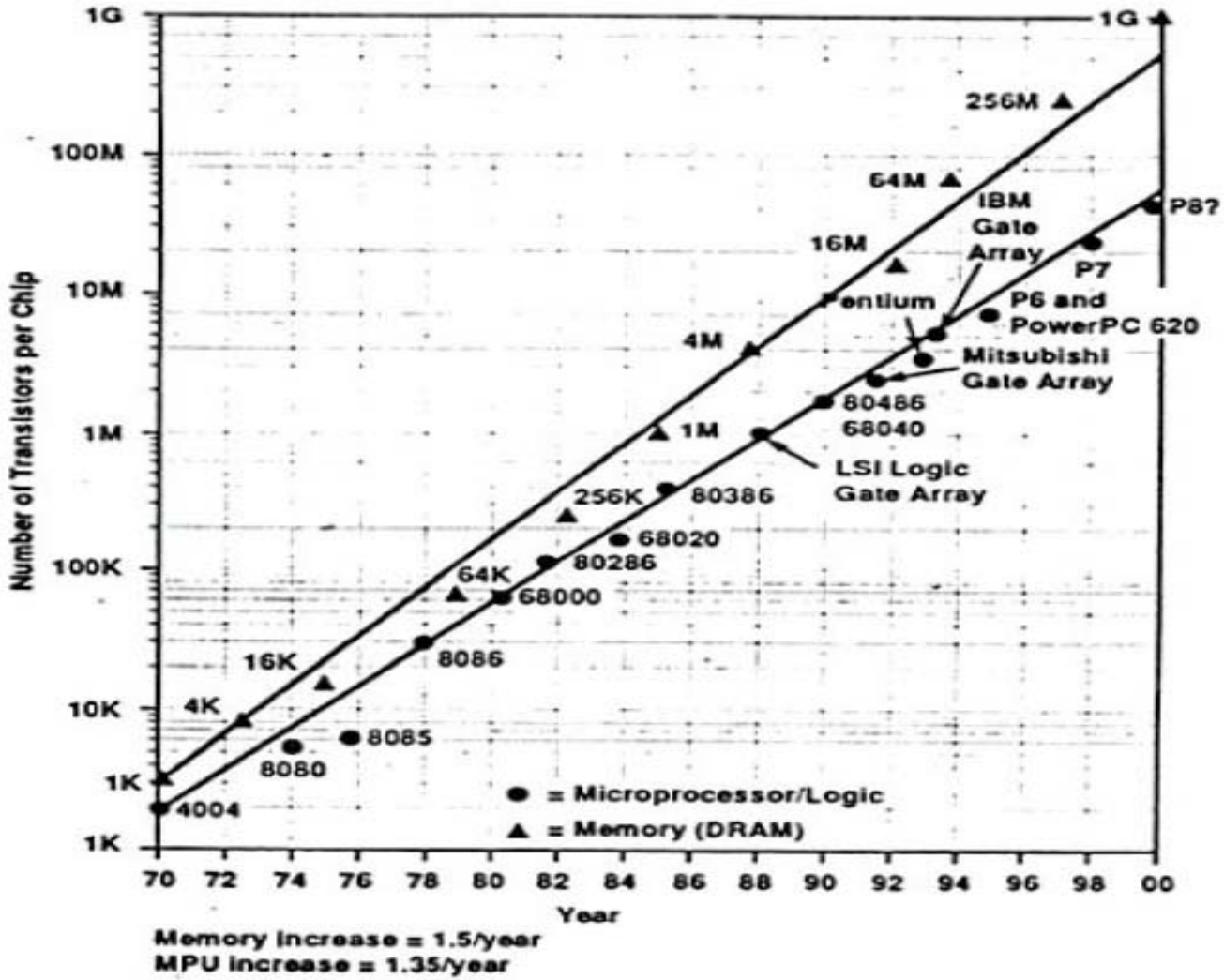
Plain View

How To Make This ?

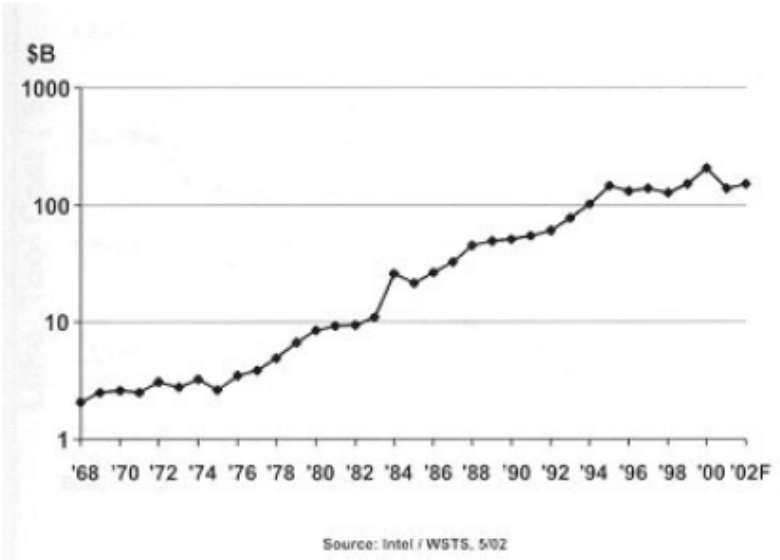
2-5. Integrated Microsystem

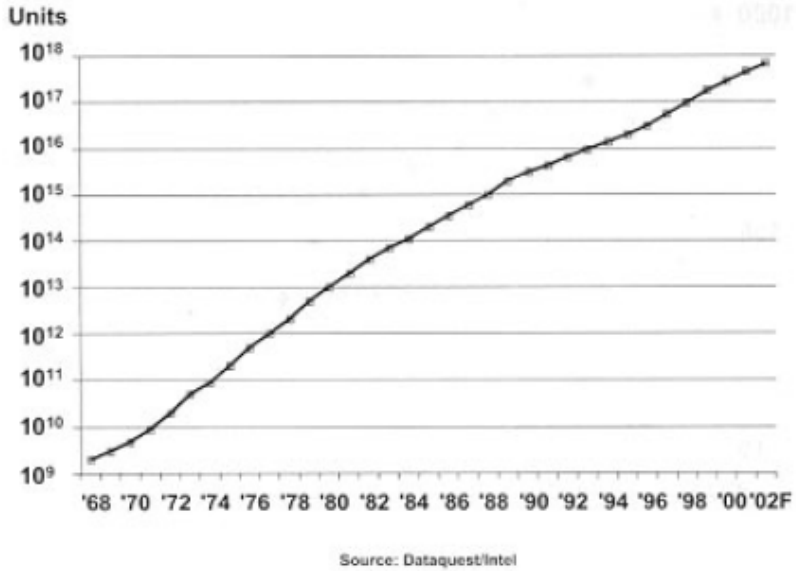


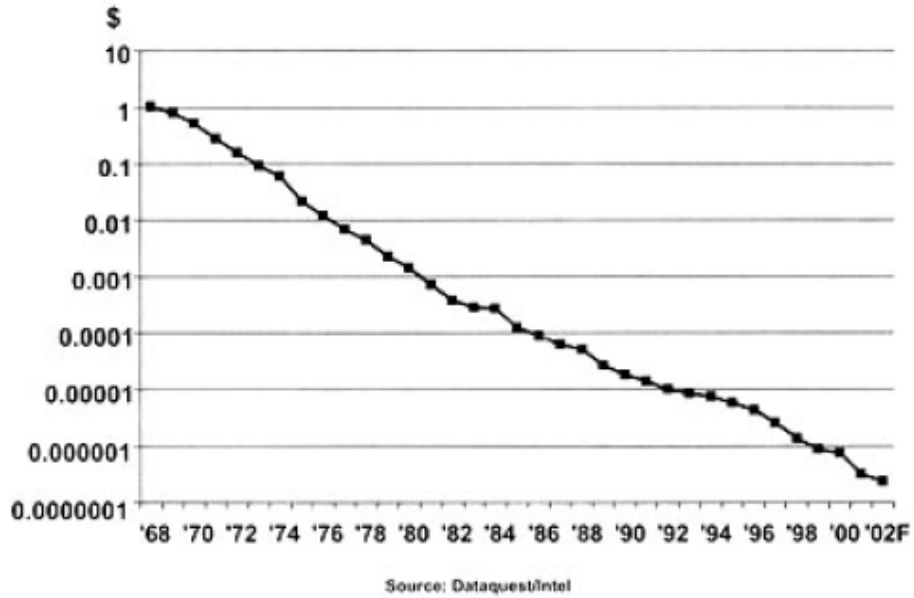
2-6. Device Density



2-7. Corollary To Moore's Law

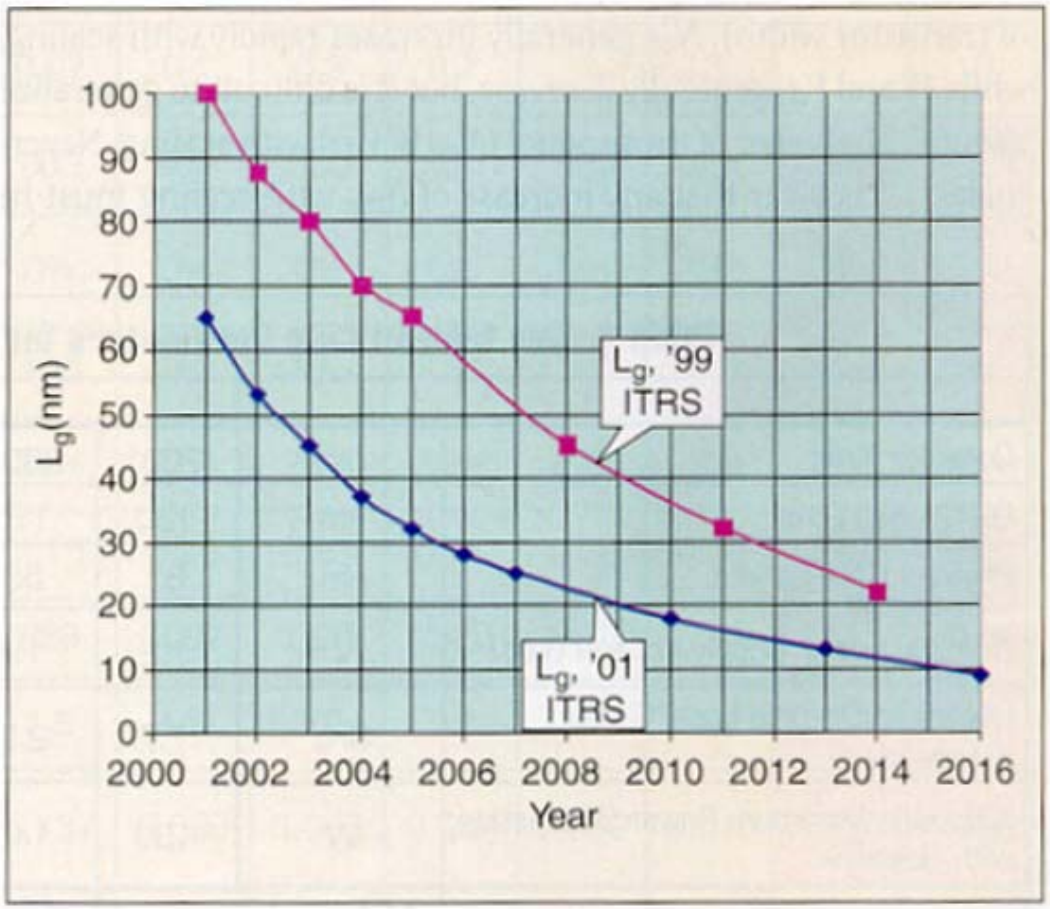






Average transistor price by year

2-8. SIA Roadmap (1999 vs. 2001)



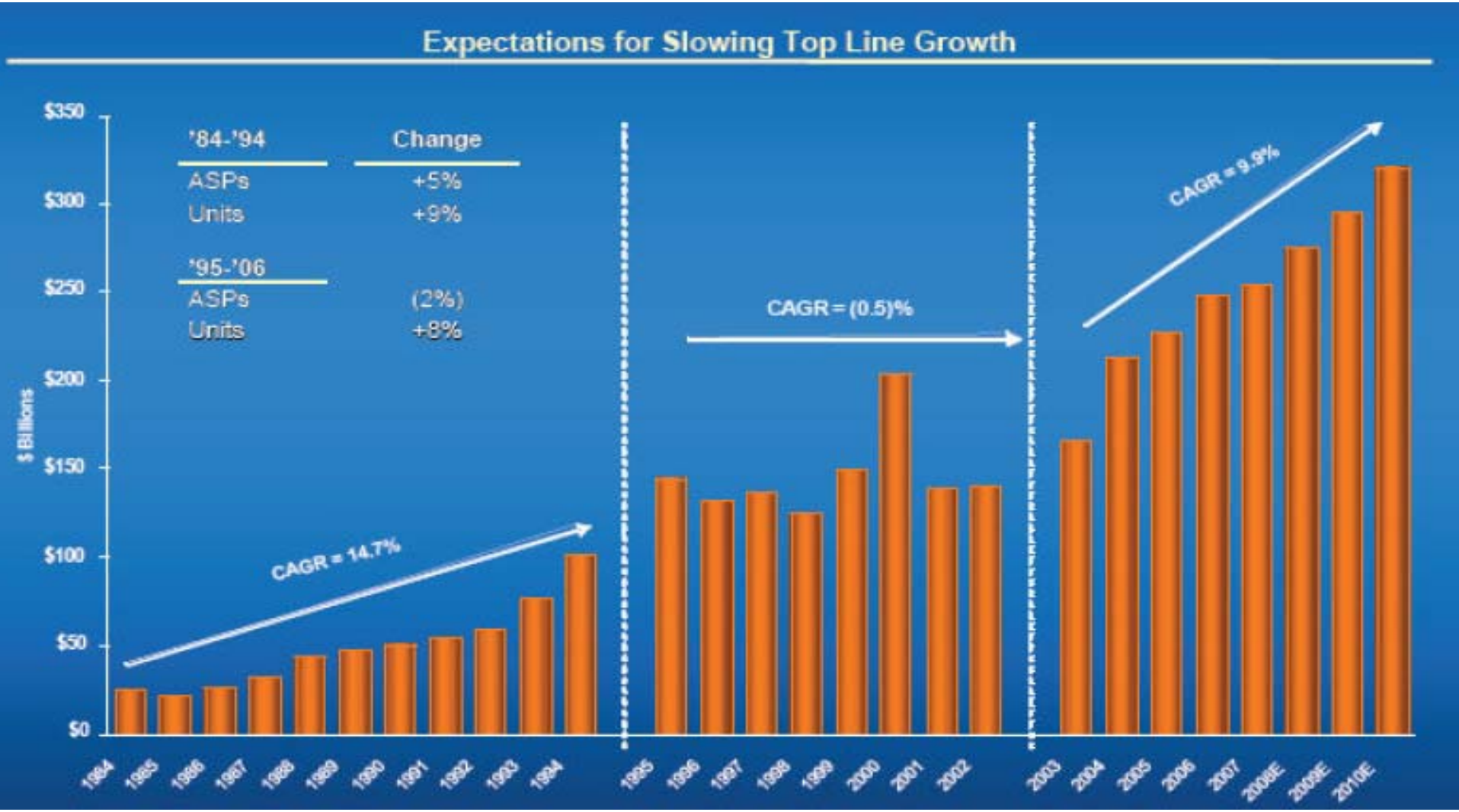
ITRS (International Technology Roadmap for Semiconductors)
Projections of physical gate length (L_g): High-performance logic

2-9. Details of 2001 ITRS Roadmap

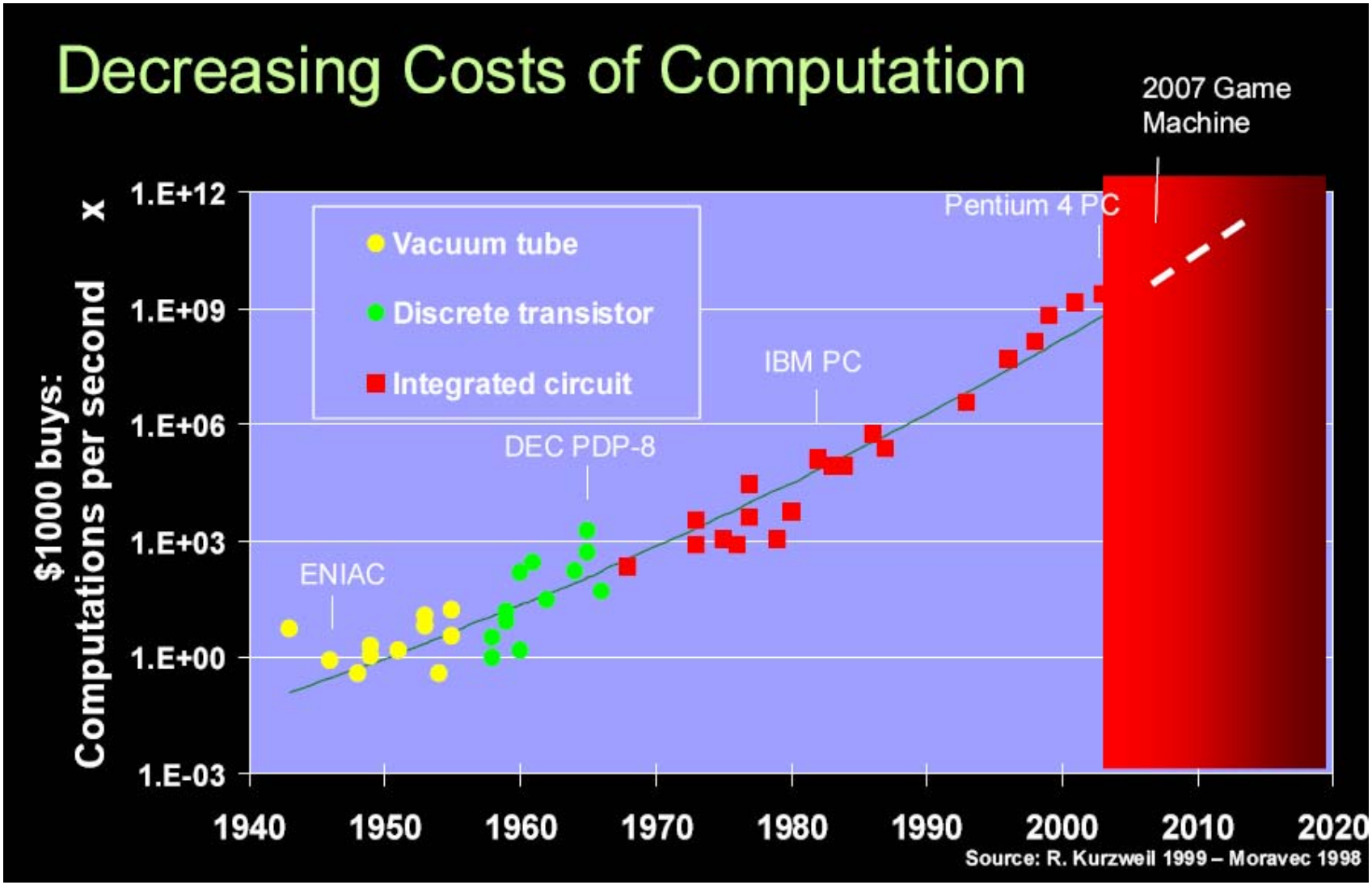
Table 2. High-Performance Logic Technology Requirements, Data from 2001 ITRS

		Near Term							Long Term		
Calendar Year		2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM Half Pitch	nm	130	115	100	90	80	70	65	45	32	22
Physical Gate Length, L_g	nm	65	53	45	37	32	28	25	18	13	9
Equivalent Oxide Thickness, T_{ox}	nm	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
Nominal Power Supply Voltage (Vdd)	V	1.2	1.1	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
Nominal High-Performance NMOS Sub-Threshold Current (@25C)	μA/μm	0.01	0.03	0.07	0.1	0.3	0.7	1	3	7	10
Nominal NMOSFET Saturation Drive Current, I_{on}	μA/μm	900	900	900	900	900	900	900	1200	1500	1500
Required Percent Current-Drive "Mobility/Transconductance Improvement"		0%	0%	0%	0%	0%	0%	0%	30%	70%	100%
Parasitic Series S/D Resistance, $R_{sd,series}$	Ω-μm	190	180	180	180	180	170	140	110	90	80
Parasitic Capacitance Percent of Ideal Gate Capacitance		19%	22%	24%	27%	29%	32%	27%	31%	36%	42%
NMOSFET Intrinsic Transistor Delay, τ_i	ps	1.65	1.35	1.13	0.99	0.83	0.76	0.68	0.39	0.22	0.15
NMOSFET Intrinsic Transistor Switching Frequency, $f_i = 1/\tau_i$	GHz	606	742	888	1007	1205	1320	1463	2570	4445	6514
Relative Device Performance		1.0	1.2	1.5	1.6	2.0	2.1	2.5	4.3	7.2	10.7
Energy per (W/Lgate=3) Device Switching Transition (Cgate*(3*Lgate)*V^2)	fJ/Device	0.347	0.212	0.137	0.099	0.065	0.052	0.032	0.015	0.007	0.002
Static Power Dissipation Per (W/Lgate=3) Device	Watts/Device	5.6E-09	6.7E-09	1.0E-08	1.1E-08	2.6E-08	5.3E-08	5.3E-08	9.7E-08	1.4E-07	1.1E-07

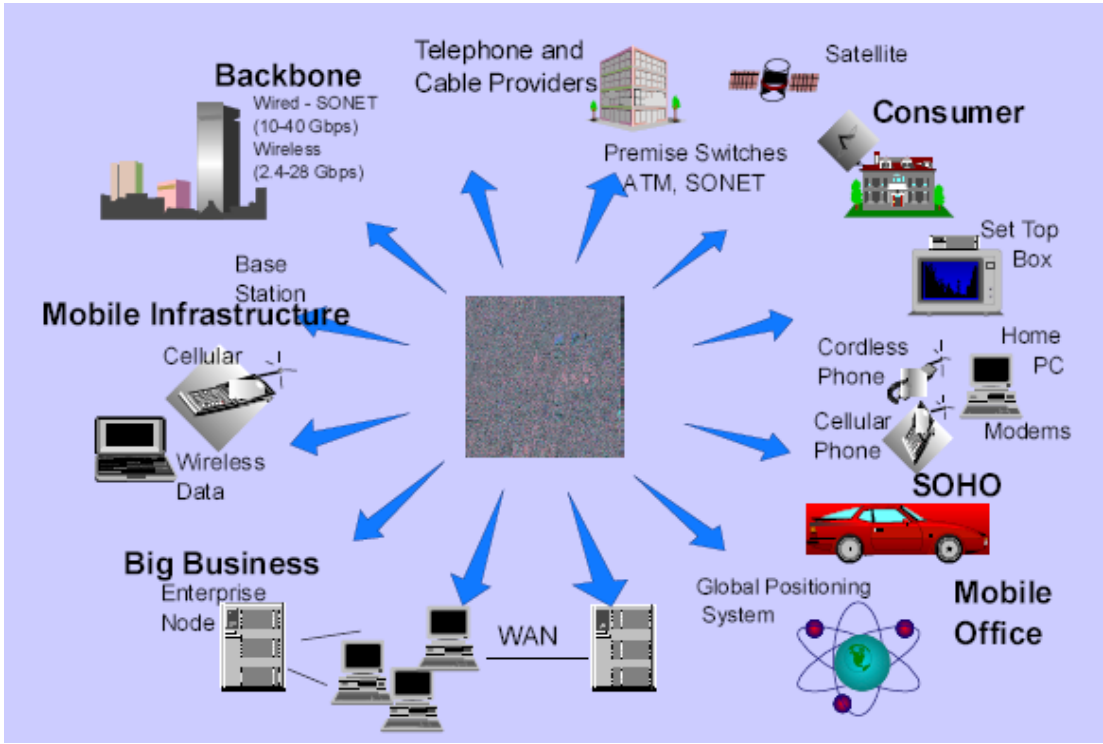
2-10. World-wide Semiconductor Market



2-11. Decreasing Costs of Computation



2-12. Chip tech. is changing the world & entering almost all facets of modern life



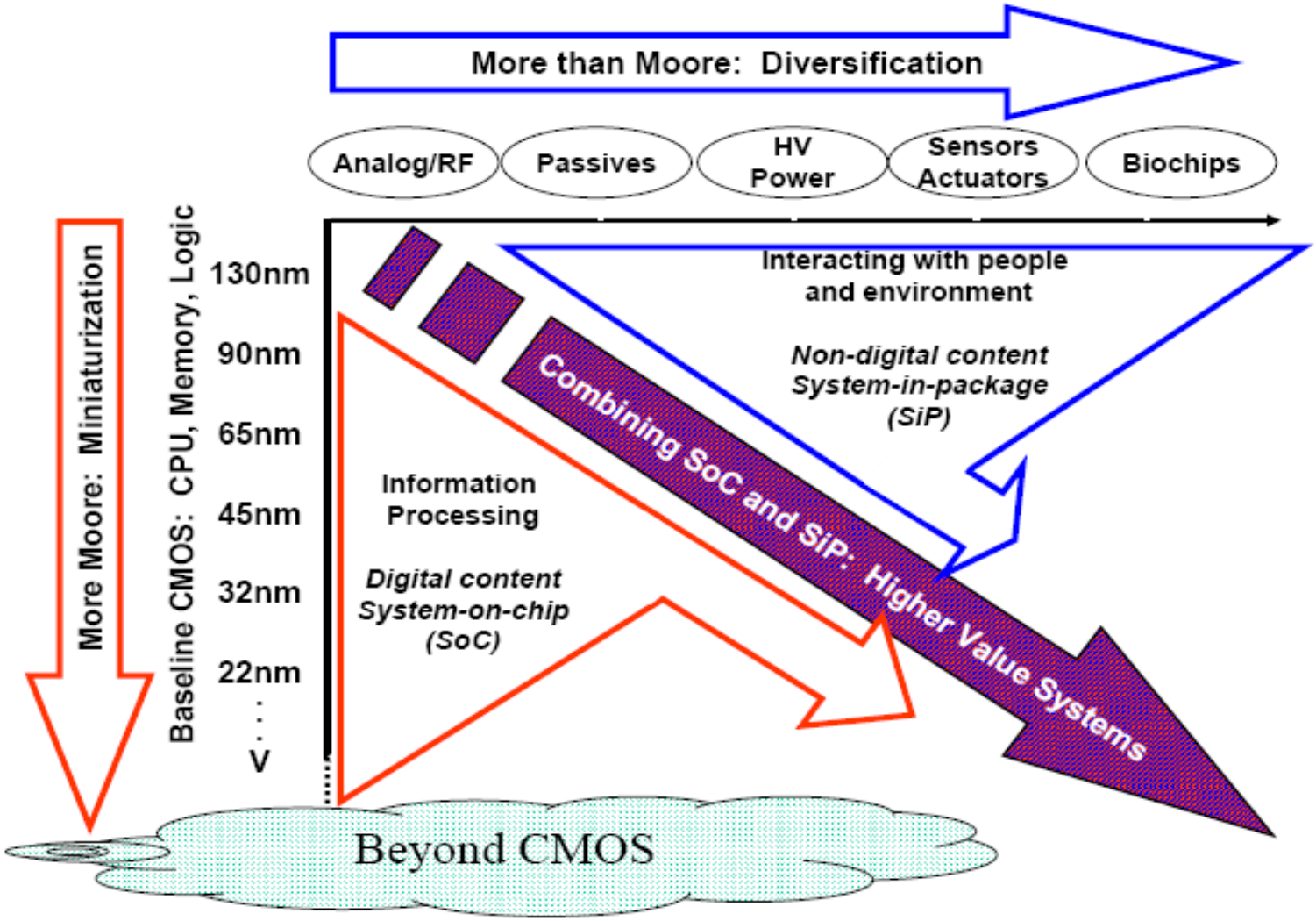
❖**How has this happened?**

❖**→technological changes**

❖**→technology generation**

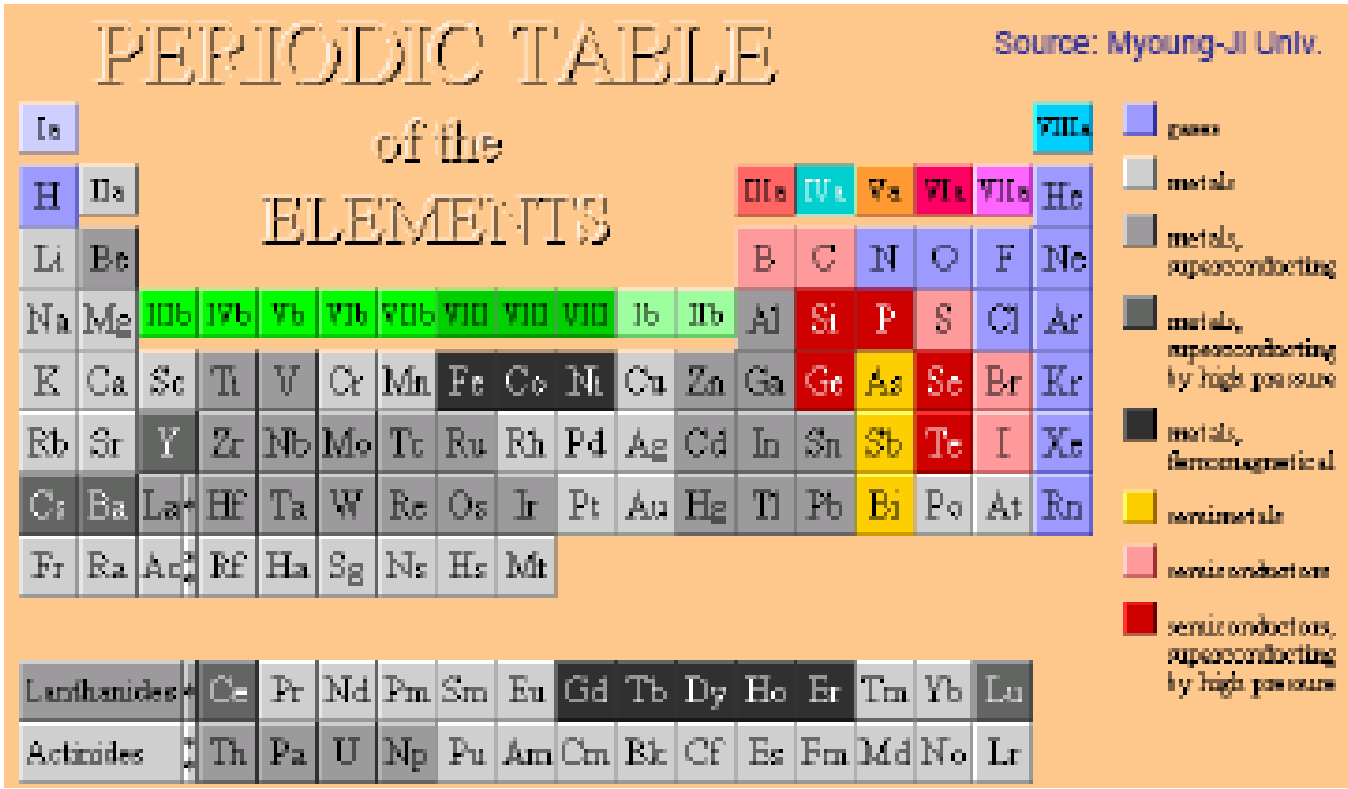
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2-13. More Than Just Scaling



3. Si Material

3-1. Periodic Table of the Elements



- Semiconductors
  - Si, SiGe, GaAs, AlGaAs, InP, HgCdTe, …

3-2. Silicon is…



- Abundant in Earth (Cost Effective)
- Commercially Available in Wafer Form
- High Modulus of Elasticity - Same As Steel
- Low Density - Same As Aluminum
- High Tensile Yield Strength - Stronger Than Steel
- Good Thermal Conductivity
- High Sensitivities to Physical Variables
- Easy to Create Passivation Layer (SiO_2)

3-3. Silicon is…(Cont.)



- Germanium
  - One of the first materials.
- Silicon
  - The dominant material today.
  - Can easily be oxidized :
    - A high-quality insulator
    - An excellent barrier layer
  - A very abundant element, a low-cost, a wider bandgap than Ge, and can operate at higher temperatures.

3-3. Silicon is…(Cont.)



- Silicon
  - Have reached integration levels of several billion components on a 20 mm × 20 mm die.
  - 1 Gbit DRAM has more than 10^9 transistors + more than 10^9 capacitors + millions of transistors in the access and decoding circuitry : 0.13 & 0.18 μm technology.
  - Provided manufacturable processes for submicron dimensions.
  - Early fabrication used the wafers which had 1- and 2-in. diameters. The size of the wafers has steadily increased 4-, 5-, 6-, 8-, and 12-in. 450 mm wafers are projected to be in use by the end of the decade.
  - 350 μm < wafer thickness < 1250 μm
  - The larger the diameter of the wafer, the more dice can be produced

3-4. Mechanical Properties of Si

	Yield Strength (10^{10} dyne/cm^2)	Knoop Hardness (kg/mm^2)	Young's Modulus (10^{12} dyne/cm^2)	Density (gm/cm^3)	Thermal Conductivity (W/cm°C)	Thermal Expansion (10^{-6}/°C)
Diamond	53	7000	10.35	3.5	20	1.0
SiC	21	2480	7.0	3.2	3.5	3.3
TiC	20	2470	4.97	4.9	3.3	6.4
Al_2O_3	15.4	2100	5.3	4.0	0.5	5.4
Si_3N_4	14	3486	3.85	3.1	0.19	0.8
Iron	12.6	400	1.96	7.8	0.803	12
SiO_2	8.4	820	.073	2.5	0.014	0.55
Si	7.0	850	1.9	2.3	1.57	2.33
Steel (max strength)	4.2	1500	2.1	7.9	0.97	12
W	4.0	485	4.1	19.3	1.78	4.5
Stainless Steel	2.1	660	2.0	7.9	0.329	17.3
Mo	2.1	275	3.43	10.3	1.38	5.0
Al	0.17	130	0.7	2.7	2.36	25

3-5. Wafer Size Evolution

- Wafer size
  - Processing costs : relatively wafer size-independent, so the die cost is lower for large wafers.

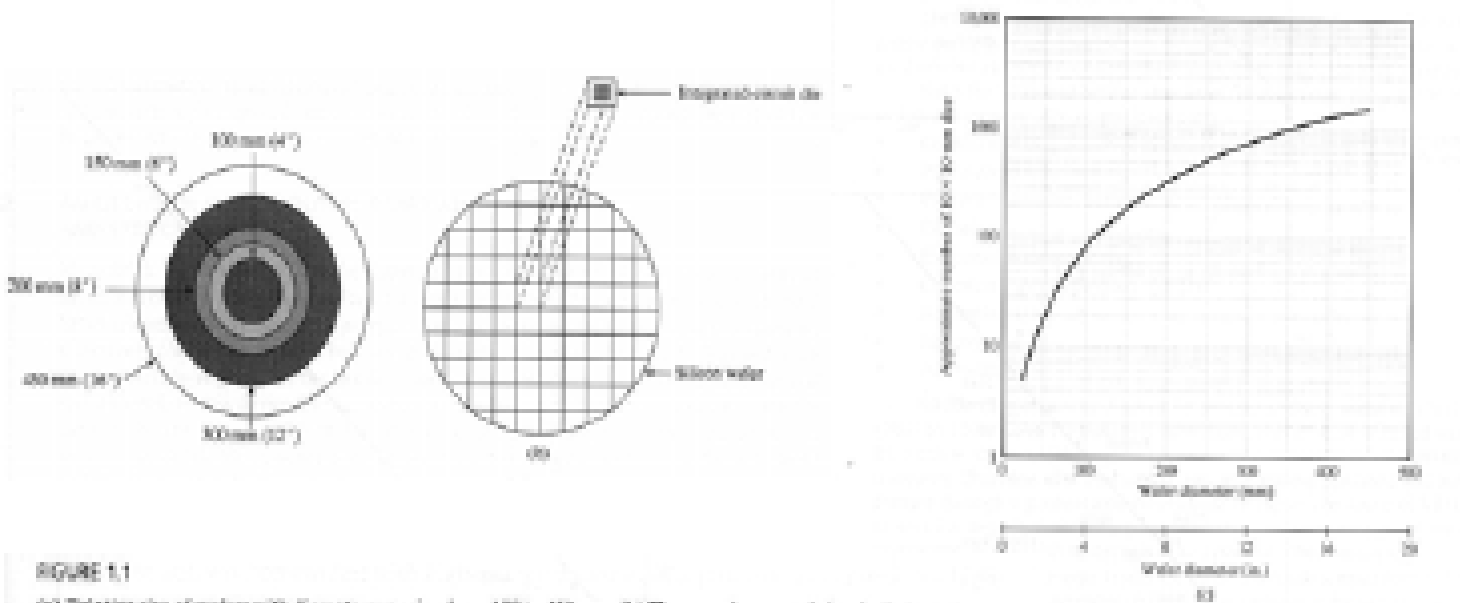


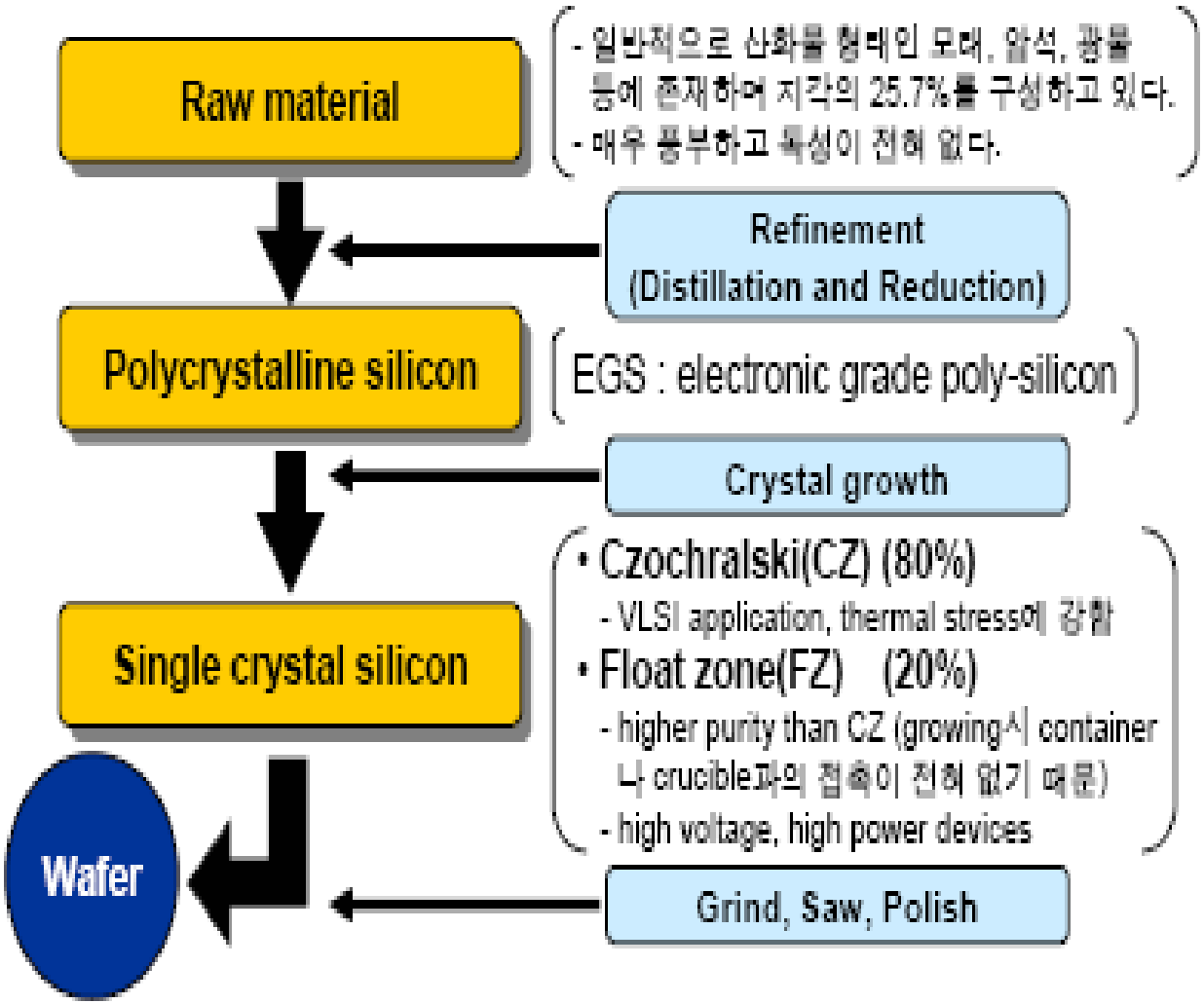
FIGURE 1.1

(a) Relative size of wafers with diameters ranging from 150 to 450 mm; (b) The same integrated circuit die is repeated hundreds of times on a typical silicon wafer; (c) the graph gives the approximate number of 10 x 10 mm dice that can be fabricated on wafers of different diameters.



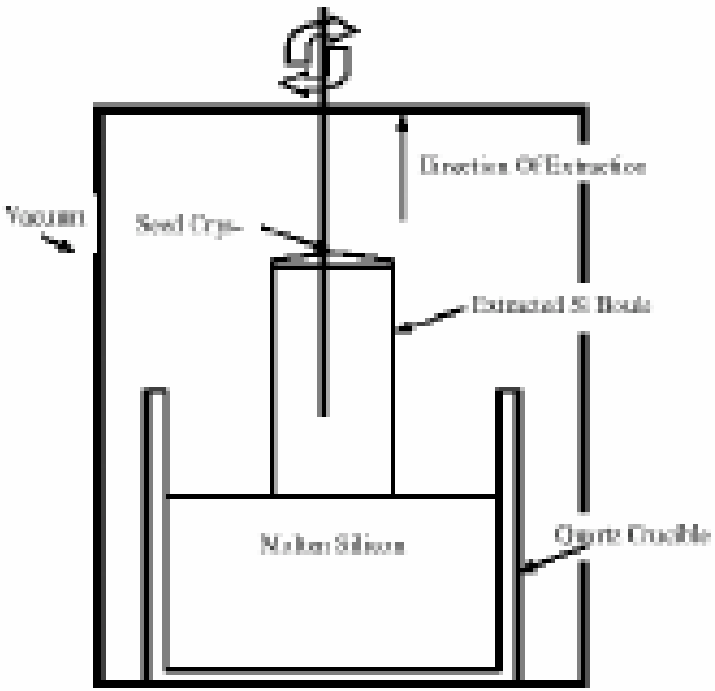
4. How To Make Wafer

4-1. Manufacturing of Single Crystal Si



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4-2. Czochralski Method of Growing



Casting: To obtain the properties we desire, high purity silicon ingots are not cast in the traditional metallurgical sense. Rather, they are grown, most typically using the Czochralski (CZ) method of crystal growing. CZ casting entails melting silicon in a quartz crucible in an inert atmosphere. Over the liquid pool of silicon, a specially prepared seed crystal is mounted on a rotating rod. This seed crystal is lowered until it just comes in contact with the surface of a molten pool of silicon. When the seed crystal comes in contact with the liquid silicon, a combination of liquid surface tension and capillary action act to form a shoulder where solidification occurs. The seed crystal's structure is replicated in the solid. Initially solidification is both radial and parallel to the normal. By precise control of extraction rate, the diameter of the solidifying crystal is established. After the desired diameter is obtained, unidirectional solidification occurs. The solidified ingot is called a boule. Once the liquid reservoir is exhausted, the length of the boule is decided.

4-3. Silicon Ingot (Boule)

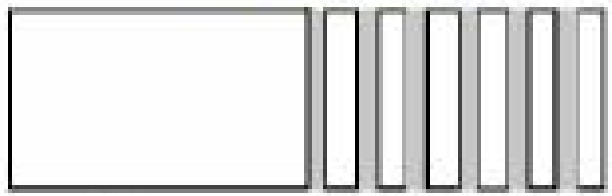


Silicon Ingot

Up to 99.999999999% pure (11 nines)

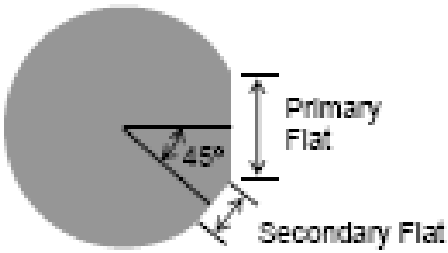
Single crystal silicon has a diamond-cubic structure: two FCC lattices displaced by .25, .25, .25.

Cutting and Polishing

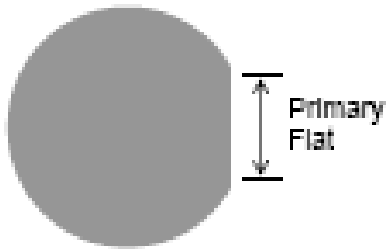


Represents Kerf Loss

4-4. Identifying Miller Indices

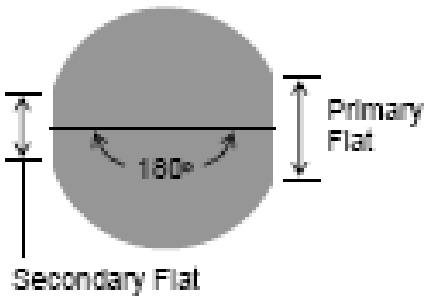


{111} n - type

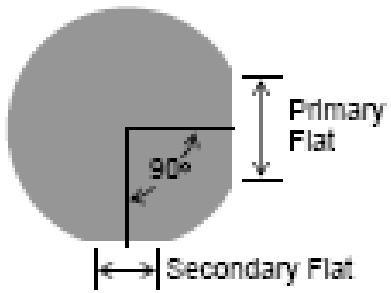


{111} p - type





{100} n - type



{100} p - type

4-5. Kinds of Wafer

★ Polished wafer

- 가장 일반적인 웨이퍼, 다결정 실리콘을 단결정 원형봉으로 만들어 이를 일정한 두께로 절단하고 연마, 식각, 경면가공, 세정의 공정을 거쳐 생산된다.

★ Epitaxial wafer

- 기존의 실리콘 웨이퍼 표면 위에 또다른 단결정층을 성장시킨 웨이퍼

★ SOI wafer

- 실리콘 웨이퍼 속에 절연박막을 삽입시킨 개념으로 실리콘 웨이퍼 기판 위에 절연막이 있고 다시 그 위에 집적회로가 제작될 단결정 실리콘 필름이 있는 것

★ Diffused wafer

- 실리콘 웨이퍼를 Furnace 내에서 dopant를 확산시켜 웨이퍼 양면에 증착 시킨 후 한 면을 연마한 웨이퍼

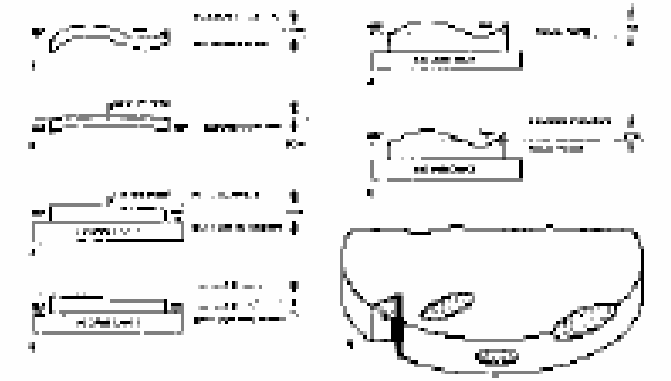
★ Hi wafer

- 실리콘 웨이퍼를 고순도의 수소가스 분위기 중에서 고온처리를 한 것으로 실리콘 웨이퍼 표면의 산소농도를 아주 작게 하여 결정결함을 거의 없앤 것.

4-6. Wafer Flatness Parameters

Parameter	100mm	125mm	150mm
Diameter (mm)	100 ± 1	125 ± 1	150 ± 1
Thickness (mm)	0.5 ~0.55	0.6 ~ 0.65	0.65 ~ 0.7
Primary flat length (mm)	30~35	40 ~ 45	55~60
Secondary flat length (mm)	16~20	25 ~ 30	35 ~ 40
Bow (μm)	60	70	60
Total thickness variation (μm)	50	65	50
Surface orientation	(100) ± 1°	Same	Same
	(111) ± 1°	Same	Same

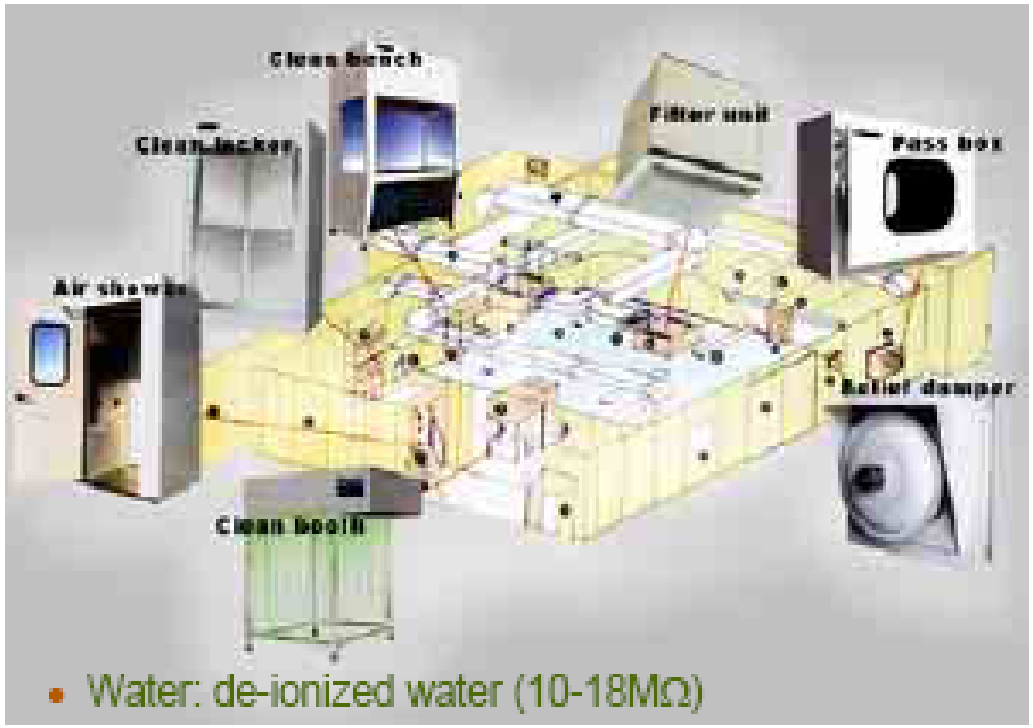
•Specifications for polished single-crystal silicon wafers



5. Overview of IC Fabrication Process

5-1. Clean room is…

- Well-Controlled Environment for Processing
  - Particle (dirt), temperature, humidity, pressure, chemical contamination, vibration, EMI
  - Expensive in building and operation



- Water: de-ionized water (10-18MΩ)

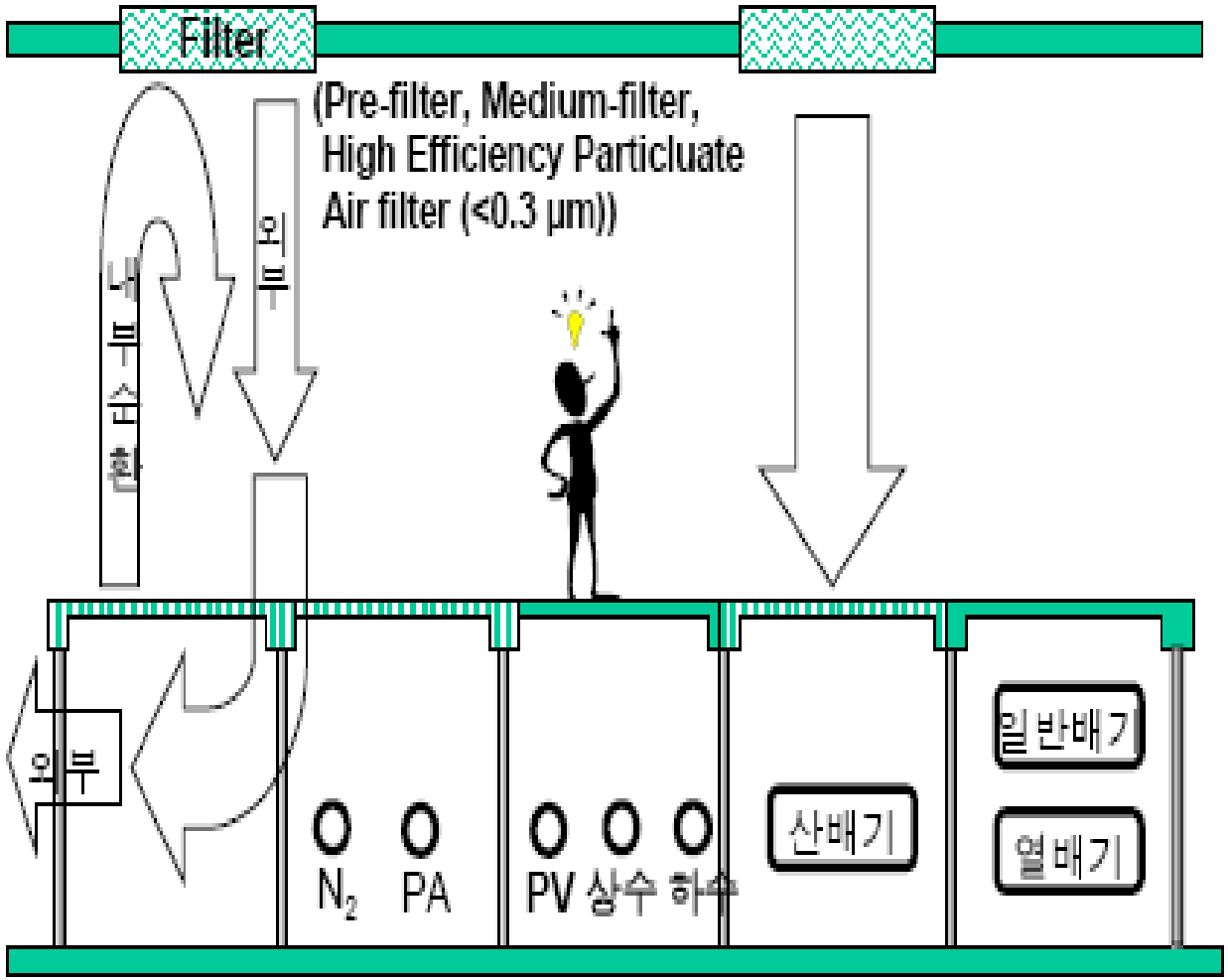
5-2. Clean room Class



청정룸 등급	입자		압력	온도			습도			기류	조도
	입경 μ	누적입자수 개/ft³	mmAq	범위 ℃	권장치 ℃	오차 ℃	최고 %	최저 %	오차 %	환기횟수	lx
등급 100	≥0.5	≤ 100	1.25 이상	19.4 ~ 25	22.2	± 2.8 특별한 경우 ±0.28	45	30	±10 특별한 경우 ± 5	층류방식 0.45m/s ±0.1m/s	1,080 ~ 1,620
등급 10,000	≥0.5 ≥5.0	≤ 10,000 ≤ 65								30 ~ 50 회/h	
등급 100,000	≥0.5 ≥5.0	≤100,000 ≤ 700								20≤ 회/h	

Class Name	0.1um	0.2um	0.3um	0.5um	5um
1(M 1.5)	35	7.5	3	1	N/A
10 (M 2.5)	350	75	30	10	N/A
100 (M 3.5)	N/A	750	300	100	N/A
1000 (M 4.5)	N/A	N/A	N/A	1,000	7
10000 (M 5.5)	N/A	N/A	N/A	10,000	70
100000 (M 6.5)	N/A	N/A	N/A	100,000	700

5-3. Clean room Structure (Example)



5-4. When You Enter Clean room

- No Particles into Clean Room
  - 음식물, 종이, 연필, 화장, 그밖에 먼지나 입자를 날릴 수 있는 일체의 것
  - Well-suited
- Being Conscious of Safety
  - Toxic & explosive gases, dangerous chemicals, heavy equipments, high power lines



Source: UCI INRF

5-4. When You Enter Clean room (Cont.)



- Wet processes for cleaning and etching : acids and bases can produce serious burns if they contact the skin, and even the fumes can produce irritation to the skin or serious eye damage.
  - Rubber gloves, an apron, and eye protection.
  - Gloves should not be relied upon to protect one during immersion in liquids, because of pinhole formation in the gloves.
- Acids and bases must not be combined during disposal.
- When diluting bases or acids, concentrated chemicals should be added to water, not the reverse.

5-4. When You Enter Clean room (Cont.)

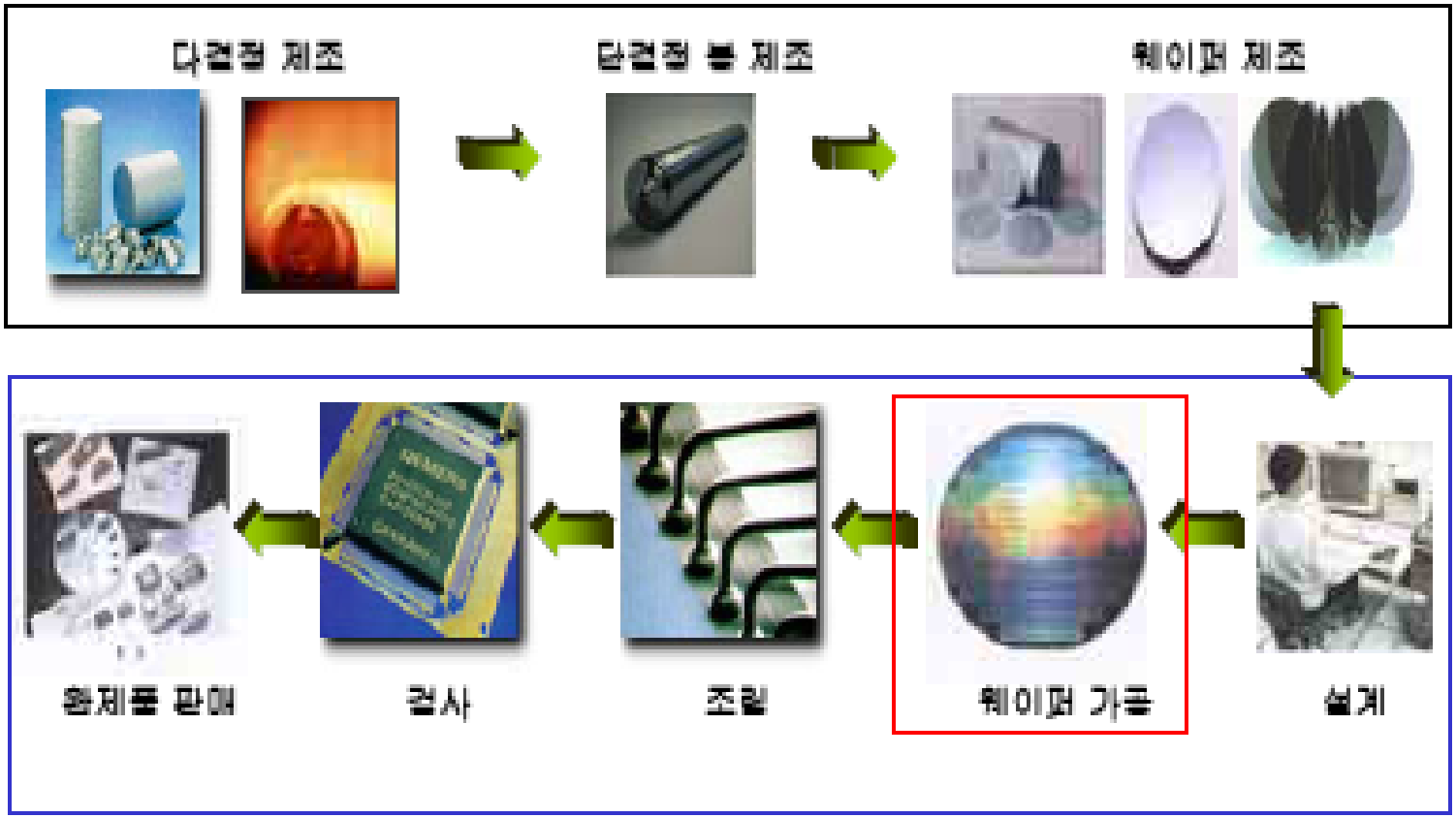


- Many acids will discolor the skin or give a burning sensation upon contact.
- HF readily penetrates the skin to produce deep and painful burns that are not detected until after the damage is done.
- I/I, LPCVD, epitaxy may involve extremely toxic or explosive gases.
- Ion implanters, plasma reactors, E-beam evaporators involve lethal voltage.

5-4. When You Enter Clean room (Cont.)

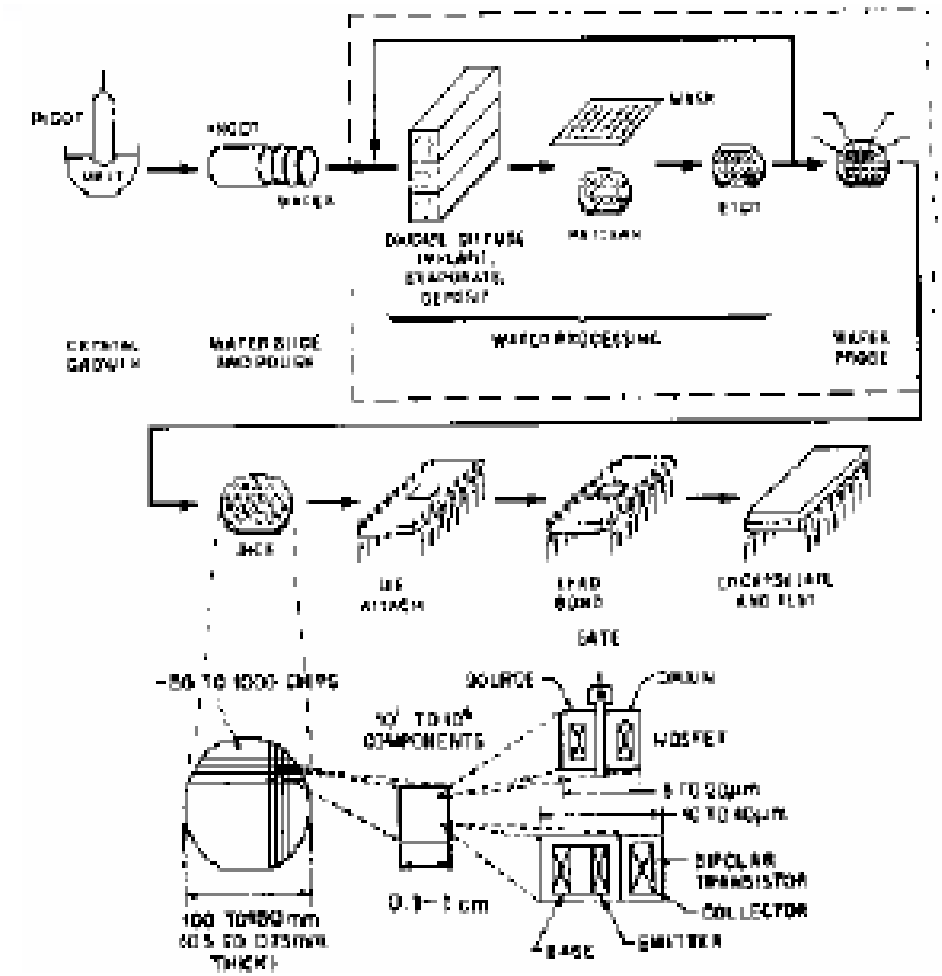


5-5. Semiconductor Fabrication Process



Dongbu Anam Semiconductor

5-6. The Whole Process Flow



- Basic process steps:
  - Oxidation
  - Photolithography
  - Etching
  - Diffusion
  - Evaporation or sputtering
  - Chemical vapor deposition (CVD)
  - Ion implantation
  - Epitaxy
  - Annealing

5-7. Basic Processes



- Oxidation
  - Silicon dioxide can be formed by heating a silicon wafer to a high temperature(1000 to 1200 °C) in the presence of oxygen
- Evaporation
  - Metal films can be deposited through evaporation by heating the metal to its melting point in a vacuum.
- Chemical vapor deposition (CVD)
  - Thin films of silicon nitride, silicon dioxide, polysilicon, and metal.

5-7. Basic Processes (Cont.)



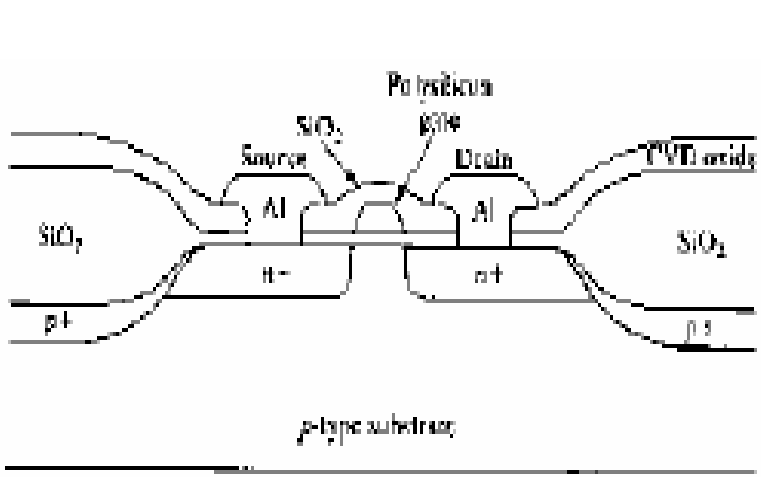
- Sputtering
  - Metal and insulators.
- Diffusion
  - Shallow n- and p-type layers are formed by high-temperature diffusion of impurities.
- Ion implantation
  - Shallow n- and p-type layers are formed by ion-implantation, in which the wafer is bombarded with high-energy ions generated in a high voltage particle accelerator

5-7. Basic Processes (Cont.)

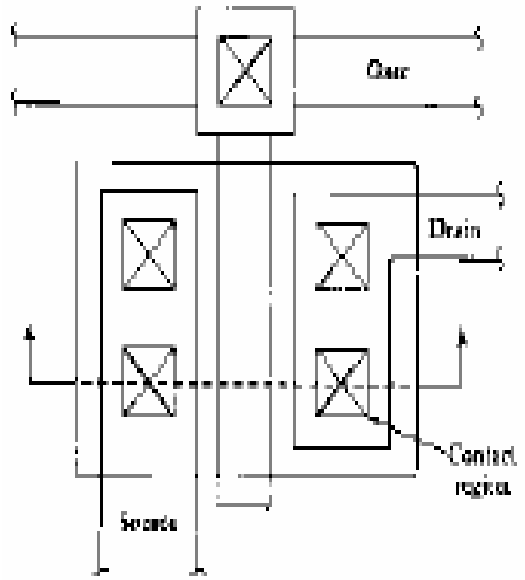


- Photolithography
  - Photolithography includes the overall process of mask fabrication and the process of transferring patterns from the masks to the wafer.
  - This process is critical to the production of integrated circuits, and the number of mask steps is often used as a measure of complexity.
  - Silicon dioxide, silicon nitride, polysilicon, photo resist can be used to mask areas of the wafer surface to prevent penetration of impurities.
  - Window patterns are transferred through the use of optical techniques.

5-8. Basic Structure of NMOS Process



Cross-Sectional View

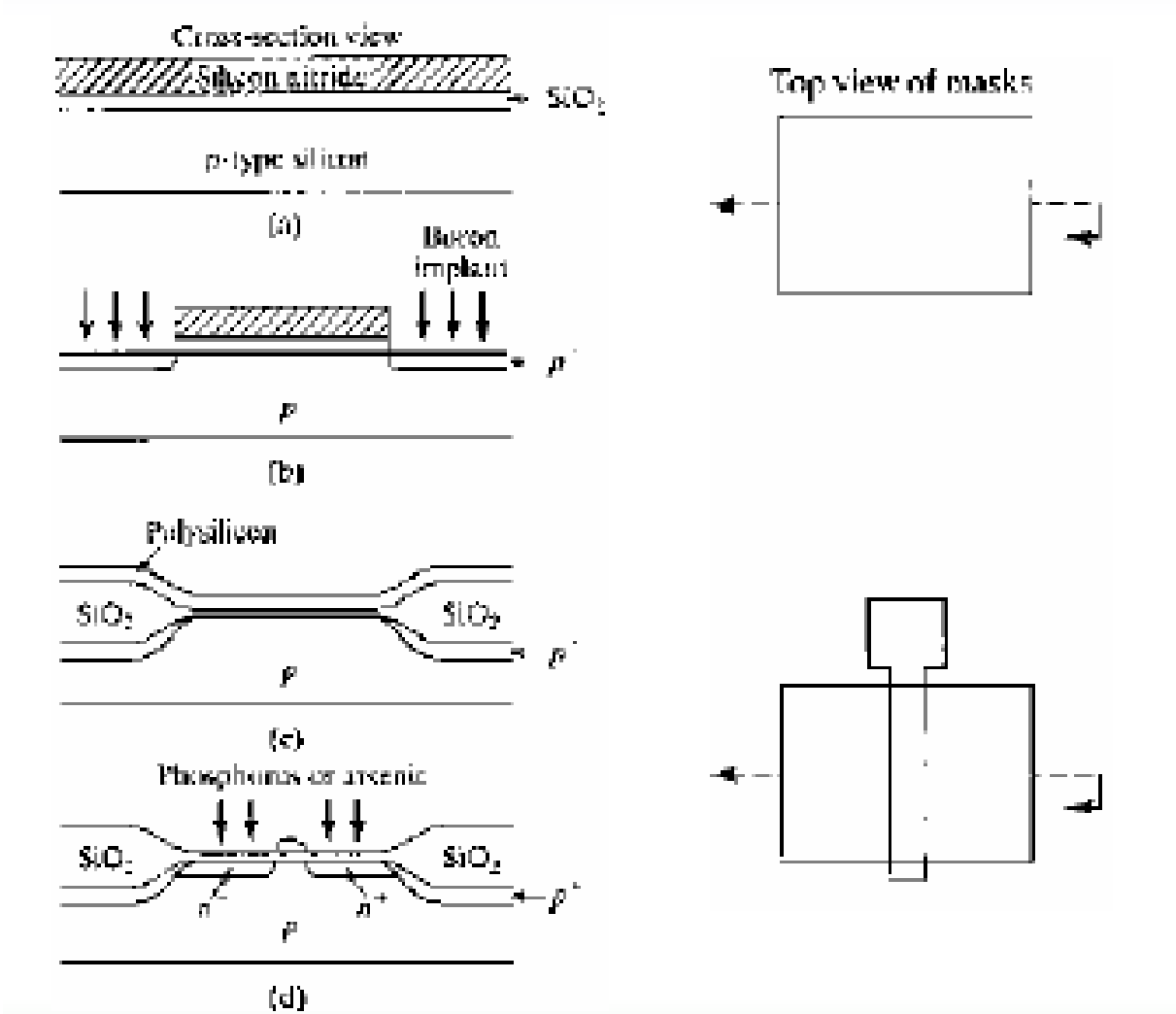


Plain View

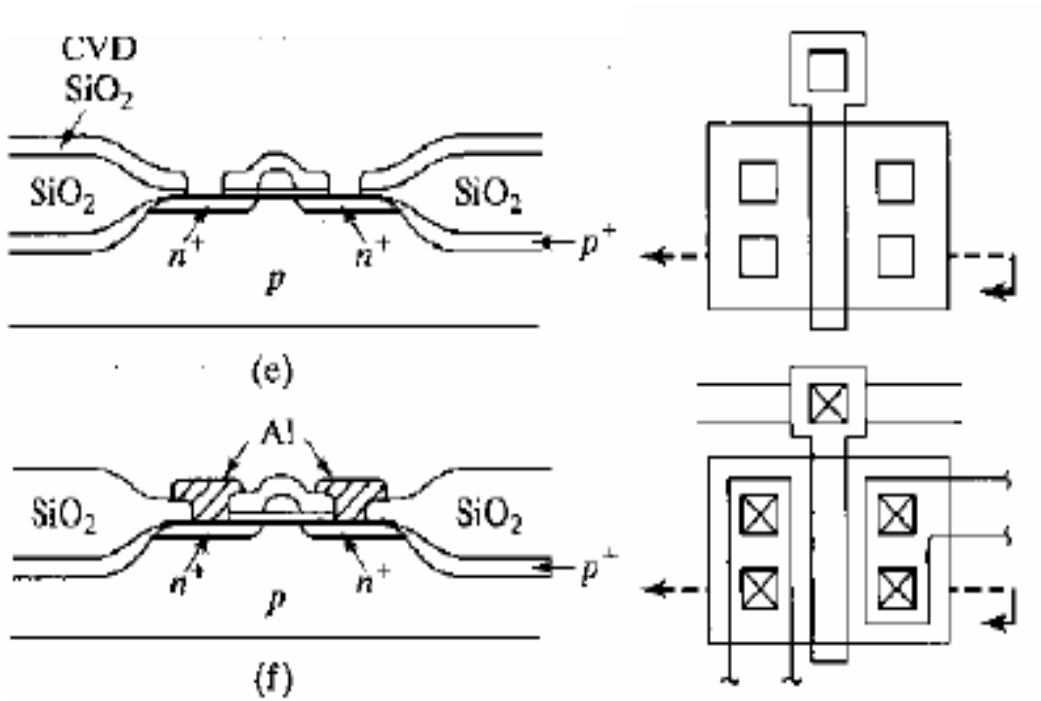
5-9. Monolithic Fabrication of NMOS Transistor

- NMOSFET is formed in a p-type substrate.
- Source/drain region are formed by selectively converting shallow region at the surface to n-type.
- Thin and thick silicon dioxide regions on the surface form the gate insulator and serve for isolation.
- Polysilicon is used to form the gate, and aluminum is used to make contact to the source and drain.
- Interconnections can be made using the diffusions, polysilicon, and metal.

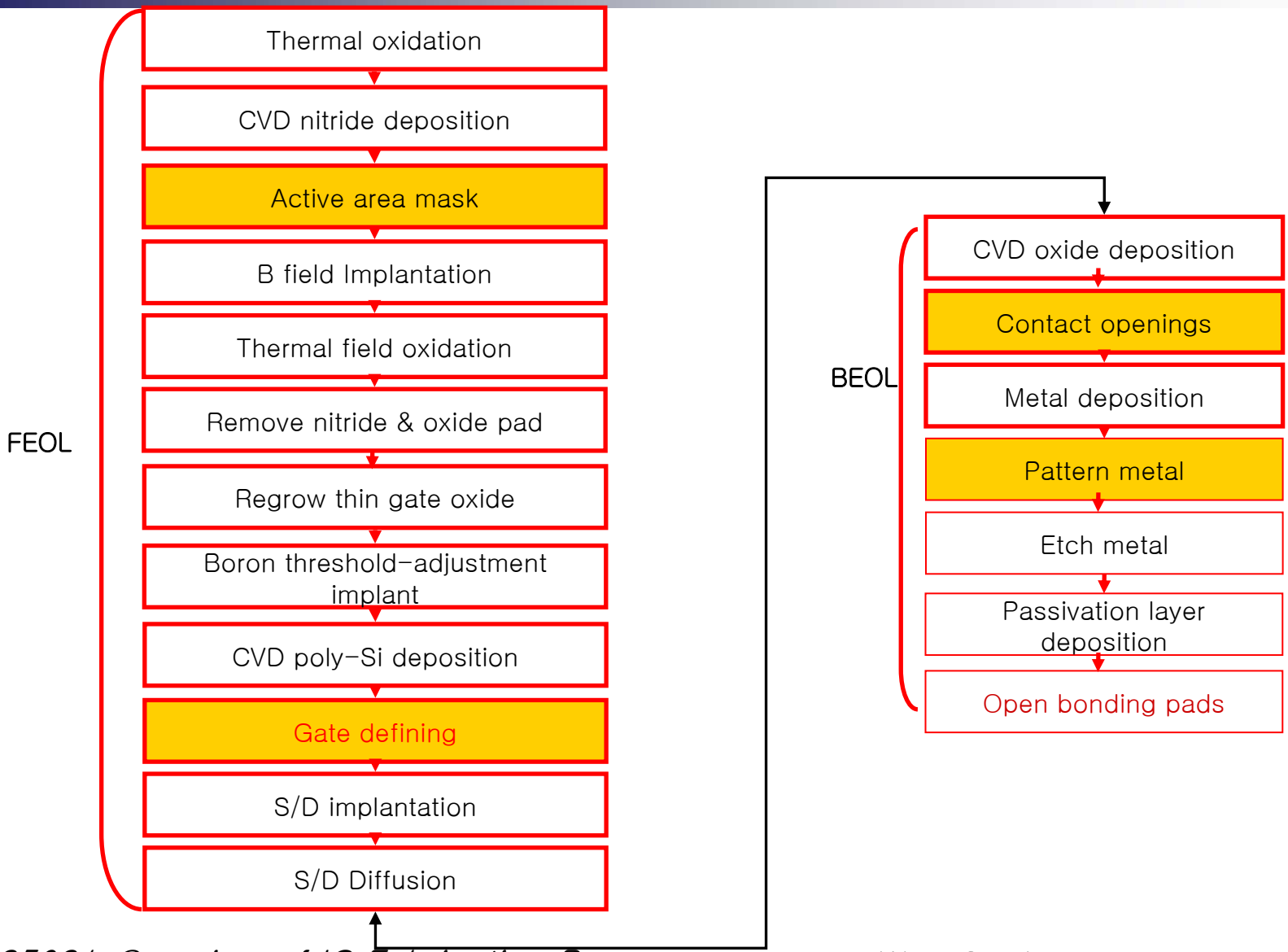
5-9. Basic NMOS Process



5-9. Basic NMOS Process (Cont.)



5-9. Basic NMOS Process Flowchart



5-10. Basic CMOS Process

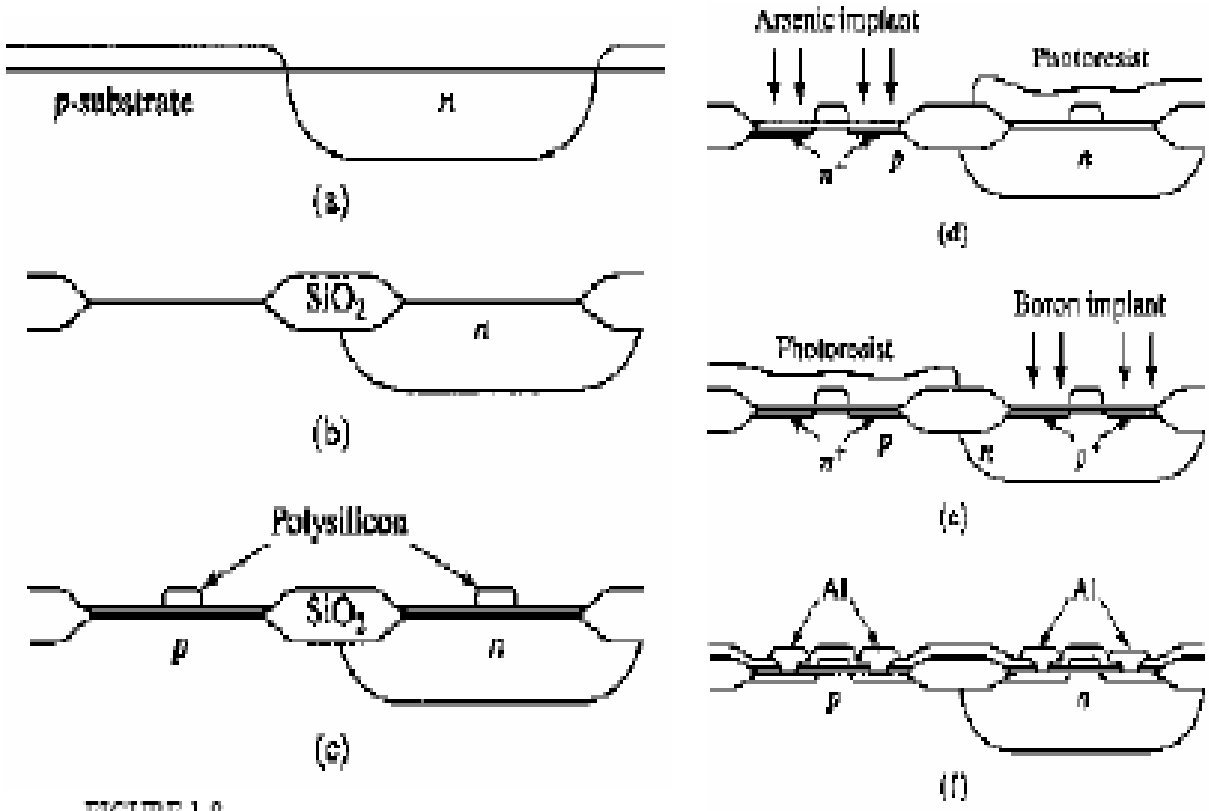


FIGURE 1.8
Cross-sectional views at major steps in a basic CMOS process.
(a) Following n-well diffusion, (b) following selective oxidation, and (c) following gate oxidation and polysilicon definition; (d) NMOS source/drain implantation; (e) PMOS source.drain implantation; (f)structure following contact and metal mask steps.

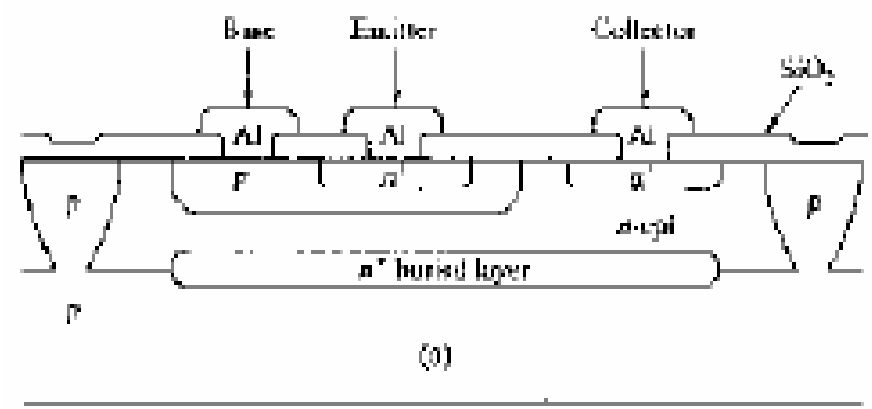
5-10. Basic CMOS Process (Cont.)

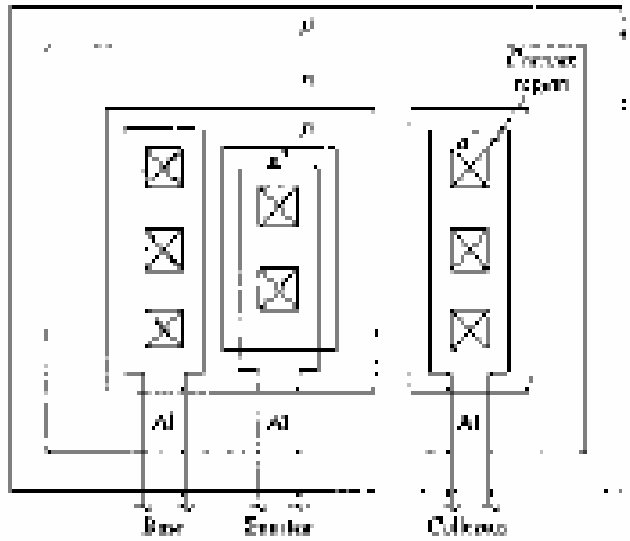


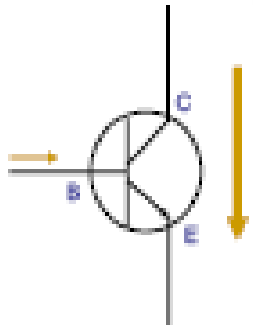
- One new mask, beyond that of the NMOS process, is used to define the "n-well" or "n-tub".
- A second new mask step is to define S/D region of the PMOSFET.
- Additional mask may be used to adjust the threshold voltage.
- Twin-well processes have been developed recently : the n- and p-channel devices can each be oprimized.
- Twin-well processes use lightly doped layers grown on heavily doped substrates to suppress latchup.

5-11. Monolithic Fabrication of Bipolar Transistor

- The basic cross section of a junction-isolated bipolar transistor



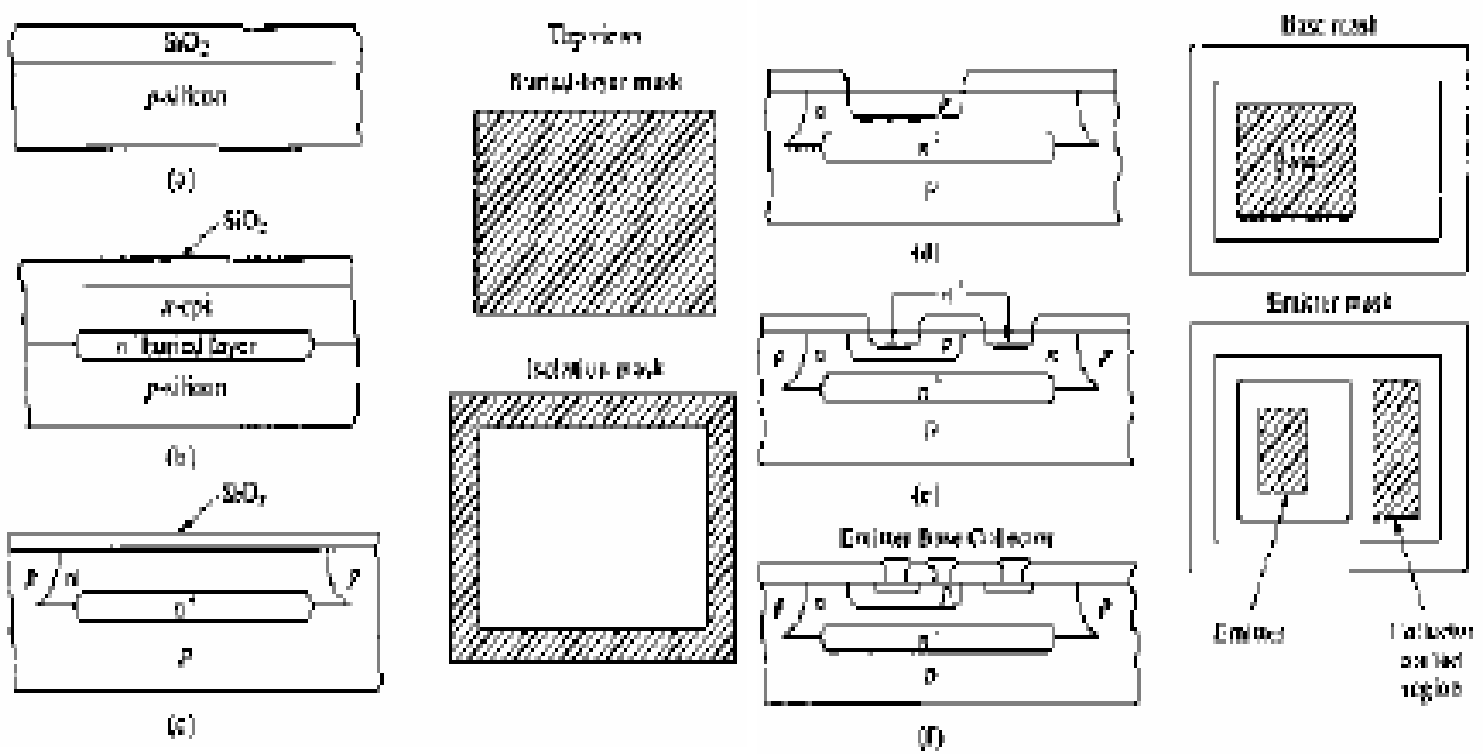




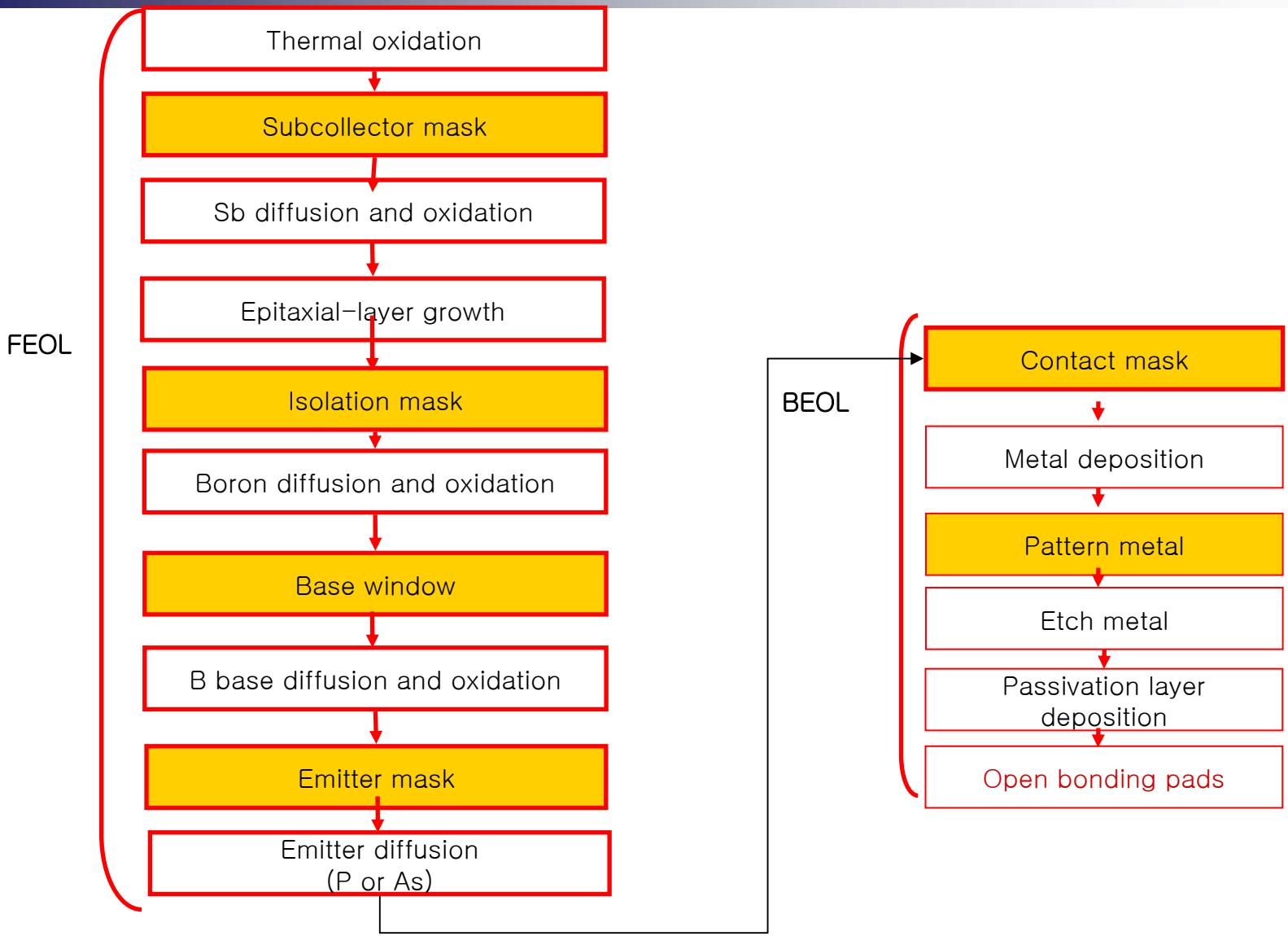
5-12. Monolithic Fabrication of NMOS Transistor

- The bipolar transistor has alternating n- and p-type regions selectively fabricated on a p-type substrate.
- Silicon dioxide is used as an insulator, and a metal is used to make electrical contact to the emitter, base, and collector.
- First mask for buried layer, or subcollector : to reduce the collector resistance.
- Epitaxy : to grow single-crystal n-type silicon. It results in a high-quality silicon layer with the same crystal structure as the original silicon wafer.

5-13. Basic Bipolar Process



5-14. Basic Bipolar Process Flowchart



35021_Overview of IC Fabrication Process : revised by Wan-Gyu Lee on September, 2008

5-15. Final Process

- After the MOS or Bipolar Process
  - Each die on the wafer is tested, and bad dice are marked with ink, sawed apart, packaging, final test, sale.

Terminology

- **MOS (Metal Oxide Semiconductor)**
- **CMOS (Complementary MOS)**
- **NMOS (n-channel MOS)**
- **VLSI (Very large-scale Integration)**
- **ITRS (International Technology Road map for Semiconductor), http://www.itrs.net**
- **SIA (The Semiconductor Industry Association)**

- **LPCVD (low-pressure chemical vapor deposition)**
- **HF (Hydrofluoric acid)**